datasheet

PRELIMINARY SPECIFICATION

1/2.8" color CMOS 1080p (1920 x 1080) HD image sensor
with PureCel®Plus and Nyxel® technologies

OS02H10

color CMOS 1080p (1920 x 1080) HD image sensor with PureCel®Plus and Nyxel® technologies

datasheet (CSP)
PRELIMINARY SPECIFICATION

version 1.1
november 2020

To learn more about OmniVision Technologies, visit www.ovt.com.

applications

- security surveillance systems
- IP cameras
- HD analog cameras

ordering information

- **OS02H10-A41A-001A-Z** (color, lead-free)
  41-pin CSP

features

- supports image sizes: 1920x1080, 960x540, 960x540, and 480x270
- supports windowing function
- supports mirror and flip functions
- supports auto black level calibration
- supports defective pixel correction
- supports black sun cancellation
- SCCB control interface for register programming
- supports high dynamic range with 2-exposure staggered HDR mode
- supports vertical 1x2 color binning and horizontal 1x2 color binning function
- supports MIPI 1-lane or 2-lane serial 10-bit/12-bit RAW image data output
- supports multi-camera synchronous function

key specifications (typical)

- **active array size:** 1920 x 1080
- **power supply:**
  core: 1.2V
  analog: 2.8V
  I/O: 1.8V
- **power requirements:**
  active: <110 mW
  XSHUTDOWN: <10 µA
- **temperature range:**
  operating: -30°C to +85°C junction temperature (see **table 6-2**)
  stable image: -20°C to +60°C junction temperature (see **table 6-2**)
- **output interfaces:** MIPI 1/2-lane / LVDS
- **output formats:** RAW10/RAW12 RGB
- **lens size:** 1/2.8"
- **lens chief ray angle:** 9° linear (see **figure 8-3**)
- **input clock frequency:** 6~27 MHz
- **maximum image transfer rate:**
  1920 x 1080: 60 fps
- **shutter:** rolling
- **sensitivity:** TBD
- **max S/N ratio:** TBD
- **dynamic range:** TBD
- **pixel size:** 2.9 µm x 2.9 µm
- **image area:** 5587.34 µm x 3153.02 µm
- **package dimensions:** 6567.7 µm x 3938.8 µm

note Power requirements specifications are estimated values and are subject to change when measured data using real silicon is available.

table of contents

1 signal descriptions **1-1**

2 system level description **2-1**

2.1 overview 2-1

2.2 architecture 2-1

2.3 format and frame 2-4

2.4 high dynamic range (HDR) mode 2-5

2.4.1 variable maximum short exposure HDR mode 2-6

2.4.2 fixed maximum short exposure HDR mode 2-6

2.5 output interface 2-6

2.5.1 MIPI interface 2-6

2.5.2 D-PHY function 2-7

2.5.3 data lane parameters 2-7

2.5.4 clock lane parameters 2-8

2.6 power up/off sequence 2-9

2.7 SCCB bus 2-12

2.7.1 single read and single write 2-12

2.7.2 data bit transfer 2-13

2.7.3 acknowledge bit 2-13

2.7.4 data valid 2-13

2.7.5 timing parameter 2-14

3 block level description **3-1**

3.1 pixel array structure 3-1

3.2 binning 3-2

3.3 10-bit A/D converters 3-3

3.4 PLL and clock generator 3-3

3.4.1 PLL1 3-3

3.4.2 PLL2 3-3

4 image sensor core digital functions **4-1**

4.1 mirror and flip 4-1

4.2 windowing 4-2

4.2.1 digital windowing 4-2

4.2.2 analog windowing 4-3

4.3 test pattern 4-6

4.4 auto black level calibration (BLC) 4-7
4.5 OTP defect pixel correction 4-11
4.6 digital gain/analog gain 4-15
4.7 exposure control 4-19
4.8 one-time programmable (OTP) memory 4-20
5 register tables 5-1
5.1 system control [P0:0x02 - P0:0x05, P0:0x1B - P0:0x71] 5-1
5.2 MIPI control [P0:0x8D - P0:0xB6] 5-6
5.3 TMS [P0:0xB7] 5-8
5.4 OSC [P0:0xF0 - P0:0xFC] 5-8
5.5 CIS control [P1:0x01 - P1:0x4F, P1:0xCD - P1:0xF2] 5-10
5.6 package [P2:0x53 - P1:0x54] 5-18
5.7 state [P2:0x55 - P2:0x5C] 5-19
5.8 dynamic DPC [P2:0x00 - P2:0x5F] 5-20
5.9 OTP BPC [P2:0x60 - P2:0x63, P4:0x12 - P4:0x15, P4:0x33 - P4:0x36] 5-24
5.10 demo_sif [P2:0xA0 - P2:0xFA, P4:0x16 - P4:0x32] 5-25
5.11 BLC [P2:0x64 - P2:0x9F] 5-28
5.12 OTP IP [P3:0xE0 - P3:0xE6] 5-33
5.13 OTP status [P3:0xE7, P3:0xEC] 5-33
5.14 OTP mode [P3:0xD0, P3:0xE8, P3:0xEA - P3:0xEB] 5-34
5.15 TPM [P6:0x00 - P6:0x23] 5-35
5.16 LVDS interface [P9:0x00 - P9:0x0E] 5-37
5.17 page selection [0xFD] 5-38
6 operating specifications 6-1
6.1 absolute maximum ratings 6-1
6.2 functional temperature 6-1
6.3 DC characteristics 6-2
6.4 timing characteristics 6-3
7 mechanical specifications 7-1
7.1 physical specifications 7-1
7.2 IR reflow specifications 7-3
7.3 PCB and SMT design recommendations 7-4
7.3.1 PCB design recommendations 7-4
7.3.2 SMT design recommendations 7-5

8 optical specifications **8-1**

8.1 sensor array center 8-1

8.2 lens chief ray angle (CRA) 8-2

list of figures

figure 1-1	pin diagram	1-1
figure 2-1	OS02H10 block diagram	2-2
figure 2-2	OS02H10 reference schematic	2-3
figure 2-3	long and short frame transmission in HDR mode	2-5
figure 2-4	variable maximum short exposure HDR mode	2-6
figure 2-5	fixed maximum short exposure HDR mode	2-6
figure 2-6	switching clock lane between clock transmission and low-power mode	2-7
figure 2-7	high-speed data transmission bursts	2-7
figure 2-8	power up sequence timing	2-9
figure 2-9	power down sequence timing	2-10
figure 2-10	SCCB read and write message description (SID pin set high)	2-12
figure 2-11	SCCB read and write message description (SID pin set low)	2-13
figure 2-12	SCCB acknowledge bit diagram	2-13
figure 2-13	SCCB data transport diagram	2-13
figure 2-14	SCCB bus timing parameter diagram	2-14
figure 3-1	pixel array region color filter layout	3-1
figure 3-2	example of horizontal 1x2 binning	3-2
figure 3-3	example of vertical 1x2 binning	3-2
figure 3-4	example of 2x2 mono binning	3-2
figure 3-5	PLL1 block diagram	3-3
figure 3-6	PLL2 block diagram	3-3
figure 4-1	mirror and flip samples	4-1
figure 4-2	digital windowing diagram	4-2
figure 4-3	full size mode	4-3
figure 4-4	binning mode	4-4
figure 4-5	test pattern diagram	4-6
figure 6-1	reference clock input timing diagram	6-3
figure 7-1	package specifications	7-1
figure 7-2	IR reflow ramp rate requirements	7-3
figure 7-3	PCB pad example	7-4
figure 7-4	tear drop design example	7-4
figure 8-1	sensor array center	8-1
figure 8-2	final image output	8-1

figure 8-3 chief ray angle (CRA) 8-2

list of tables

table 1-1 signal descriptions 1-1
table 1-2 pad symbol and equivalent circuit 1-3
table 2-1 MIPI formats and frame rates 2-4
table 2-2 data lane parameters 2-7
table 2-3 clock lane parameters 2-8
table 2-4 power up sequence requirements 2-9
table 2-5 power up sequence timing constraints 2-10
table 2-6 power down sequence requirements 2-11
table 2-7 power down sequence timing constraints 2-11
table 2-8 SCCB interface timing specifications 2-14
table 4-1 mirror and flip registers 4-1
table 4-2 digital windowing control registers 4-2
table 4-3 analog windowing control registers 4-5
table 4-4 test enable register 4-6
table 4-5 auto BLC registers 4-7
table 4-6 OTP defect pixel correction registers 4-11
table 4-7 dynamic defect pixel correction registers 4-12
table 4-8 digital gain/analog gain registers 4-15
table 4-9 register mapping relationship 4-15
table 4-10 actual analog gain 4-16
table 4-11 exposure control registers 4-19
table 5-1 system control registers 5-1
table 5-2 MIPI control registers 5-6
table 5-3 TMS register 5-8
table 5-4 OSC registers 5-8
table 5-5 CIS control registers 5-10
table 5-6 package registers 5-18
table 5-7 state registers 5-19
table 5-8 dynamic DPC registers 5-20
table 5-9 OTP BPC registers 5-24
table 5-10 demo_sif registers 5-25
table 5-11 BLC registers 5-28

table 5-12 OTP IP registers 5-33
table 5-13 OTP status registers 5-33
table 5-14 OTP mode registers 5-34
table 5-15 TPM registers 5-35
table 5-16 LVDS interface registers 5-37
table 5-17 page selection register 5-38
table 6-1 absolute maximum ratings 6-1
table 6-2 functional temperature 6-1
table 6-3 DC characteristics (-30°C < TJ < 85°C) 6-2
table 6-4 timing characteristics 6-3
table 7-1 package dimensions 7-1
table 7-2 reflow conditions 7-3
table 7-3 ball pad opening size and recommended PCB NSMD ball pad size 7-4
table 8-1 CRA versus image height plot 8-2

1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OS02H10 image sensor. The package information is shown in **section 8**.

figure 1-1 pin diagram

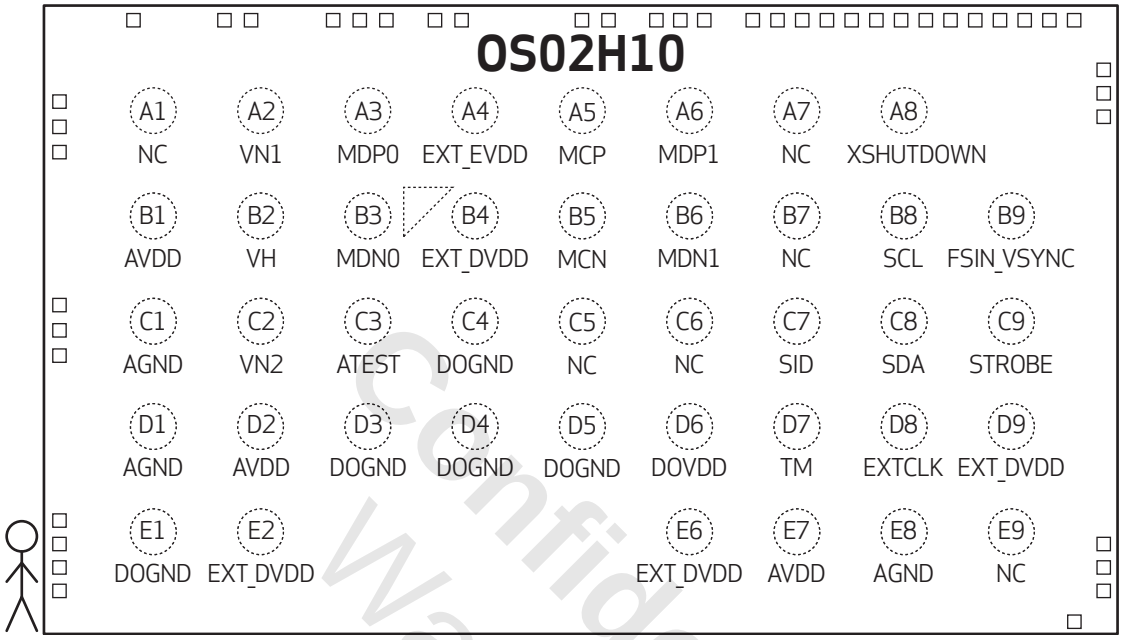


table 1-1 signal descriptions (sheet 1 of 3)

pin number	signal name	pin type	description
A1	NC	–	no connect
A2	VN1	reference	internal reference
A3	MDP0	output	MIPI data positive output
A4	EXT_EVDD	power	MIPI/PLL digital circuits
A5	MCP	output	MIPI clock positive output
A6	MDP1	output	MIPI data positive output
A7	NC	–	no connect
A8	XSHUTDOWN	input	system shutdown 0: Enable 1: Normal work

table 1-1 signal descriptions (sheet 2 of 3)

pin number	signal name	pin type	description
B1	AVDD	power	analog power, 2.8V
B2	VH	reference	internal reference
B3	MDN0	output	MIPI data negative output
B4	EXT_DVDD	power	digital circuit power, 1.2V
B5	MCN	output	MIPI clock negative output
B6	MDN1	output	MIPI data negative output
B7	NC	–	no connect
B8	SCL	input	SCCB interface input clock
B9	FSIN_VSYNC	output	video output frame start signal and frame sync
C1	AGND	ground	analog ground
C2	VN2	reference	internal reference
C3	ATEST	output	analog test pin
C4	DOGND	ground	I/O ground
C5	NC	–	no connect
C6	NC	–	no connect
C7	SID	input	sensor SCCB ID switch input 0: SCCB ID address = 0x78 1: SCCB ID address = 0x7A
C8	SDA	I/O	SCCB interface data
C9	STROBE	output	frame exposure output indicator
D1	AGND	ground	analog ground
D2	AVDD	power	analog power, 2.8V
D3	DOGND	ground	I/O ground
D4	DOGND	ground	I/O ground
D5	DOGND	ground	I/O ground
D6	DOVDD	power	I/O power, 1.8V
D7	TM	input	scan chain (active high with internal pull-down resistor)
D8	EXTCLK	input	system clock input
D9	EXT_DVDD	power	digital circuit power, 1.2V
E1	DOGND	ground	I/O ground
E2	EXT_DVDD	power	digital circuit power, 1.2V

table 1-1 signal descriptions (sheet 3 of 3)

pin number	signal name	pin type	description
E6	EXT_DVDD	power	digital circuit power, 1.2V
E7	AVDD	power	analog power, 2.8V
E8	AGND	ground	analog ground
E9	NC	–	no connect

table 1-2 pad symbol and equivalent circuit (sheet 1 of 3)

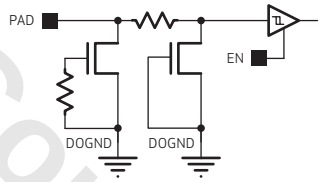
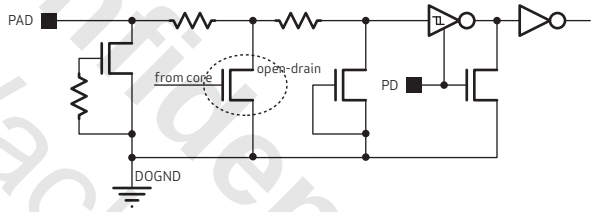
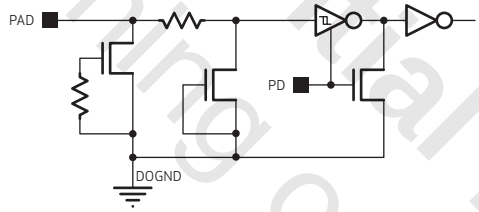
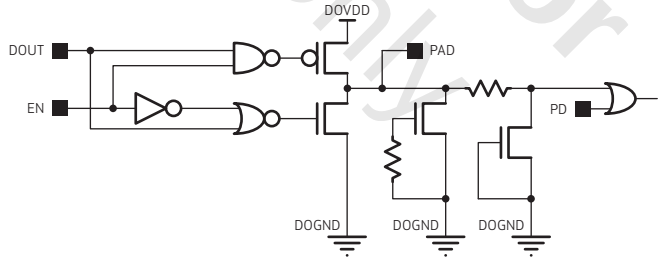
symbol	equivalent circuit
EXTCLK	
SDA	
SCL	
FSIN_VSYNC, STROBE	

table 1-2 pad symbol and equivalent circuit (sheet 2 of 3)

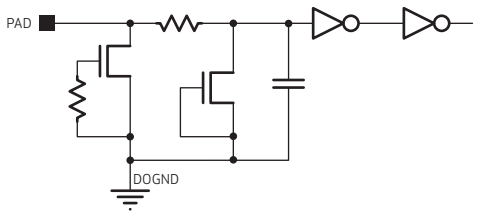
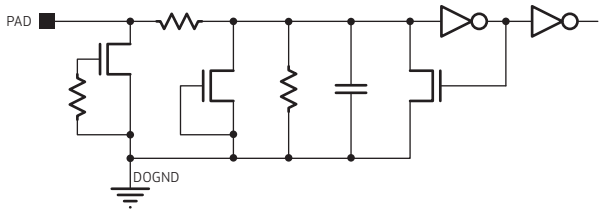
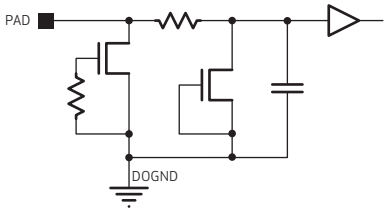
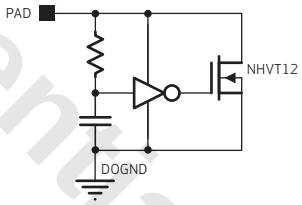
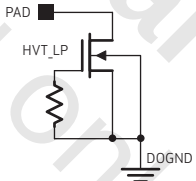
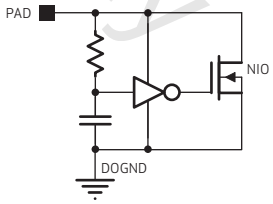
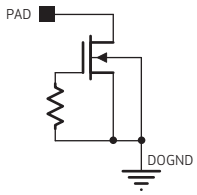
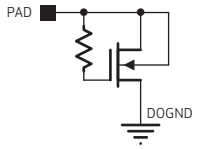
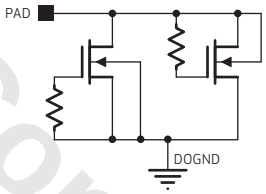
symbol	equivalent circuit
SID	
TM	
XSHUTDOWN	
EXT_DVDD, EXT_EVDD	
MCP, MCN, MDP0, MDN0, MDP1, MDN1	
AVDD, DOVDD	

table 1-2 pad symbol and equivalent circuit (sheet 3 of 3)

symbol	equivalent circuit
DOGND, VH, ATEST	
VN1, VN2	
AGND	

2 system level description

2.1 overview

The OS02H10 image sensor is a high quality, 1/2.8 inch, 1080p format, CMOS image sensor. It provides high quality digital images and high-definition (HD) video. The OS02H10 focuses on products including security surveillance systems, IP cameras and HD analog cameras.

By introducing an advanced 2.9 µm pixel architecture, the OS02H10 achieves excellent low-light sensitivity, signal-to-noise ratio, full-well capacity, quantum efficiency and low-power consumption. The default mode and programmable mode allow for a more convenient way of controlling the parameters of frame size, exposure time, gain value, etc. It also offers the following image control functions: mirror and flip, windowing, auto black level calibration, defective pixel correction, black sun cancellation, and other functions.

The OS02H10 supports a high frame rate of up to 60 fps @ 1080p format. These prominent features integrated in the OS02H10 allow for a best-in-class image sensor that will bring users vivid pictures and an excellent experience.

2.2 architecture

The OS02H10 sensor core generates streaming pixel data at a constant frame rate. **figure 2-1** shows the functional block diagram of the OS02H10 image sensor.

The timing generator outputs clocks to access the rows of the imaging array, pre-charging and sampling the rows of the array sequentially. In the time between pre-charging and sampling a row, the charge in the pixels decreases with exposure to incident light. This is the exposure time in rolling shutter architecture.

The exposure time is controlled by adjusting the time interval between pre-charging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs up to 10-bit data for each pixel in the array.

figure 2-1 OS02H10 block diagram

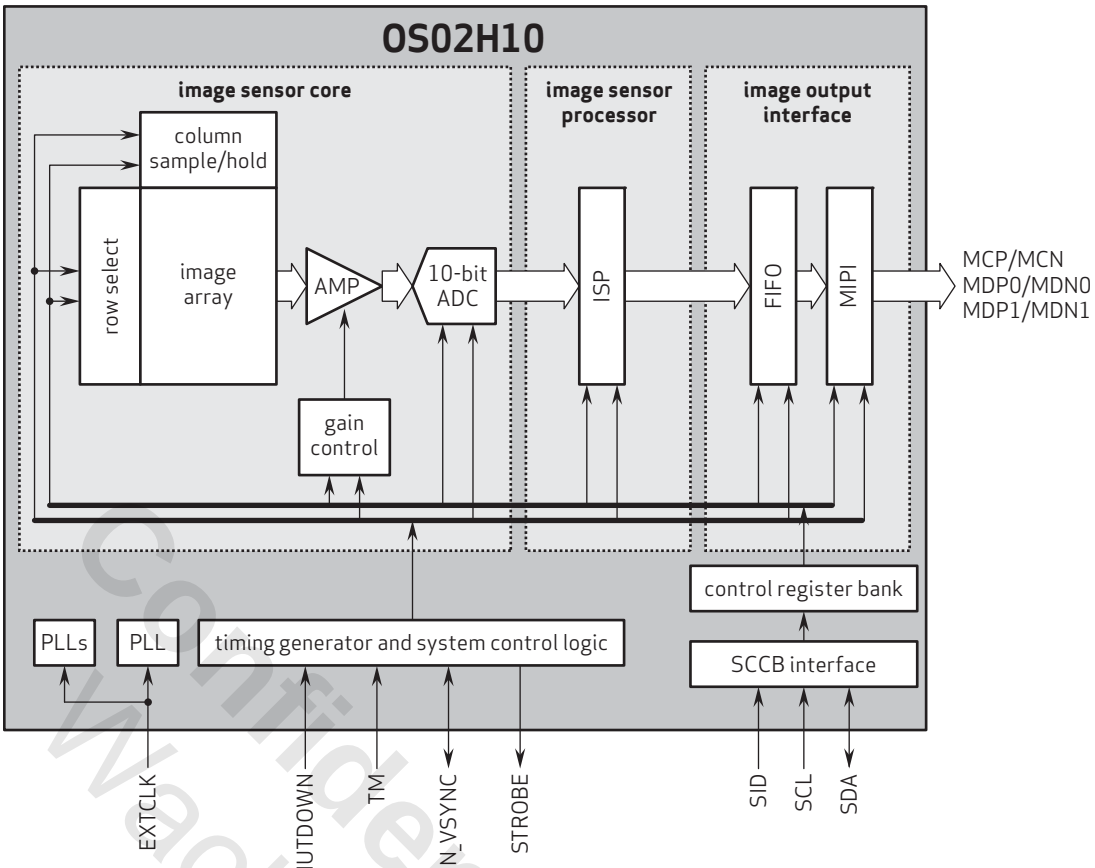
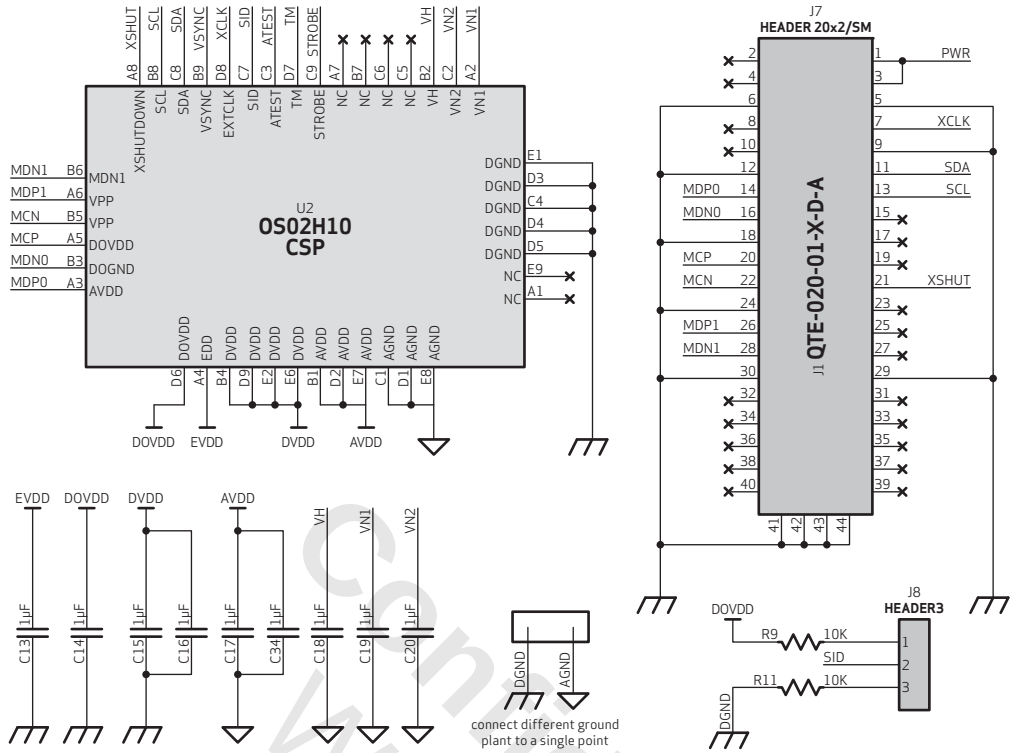


figure 2-2 OS02H10 reference schematic



note 1 client platform provides four power supplies for AVDD, DOVDD, DVDD and EVDD; AVDD is connected to 2.8V power supply, DOVDD is compatible with 1.8V power supply, DVDD is connected to 1.2V power supply, and when using MIPI interface, EVDD is connected to 1.2V power supply; VH, VN1, and VN2 are all externally connected with a 1μF capacitor and then grounded without being led out to interface.

note 2 when platform GPIO pins are limited, XSHUTDOWN must be controlled by platform GPIO.

note 3 SID is SCCB address controllable pin; when SID is connected low, write address is 0x78 and read address is 0x79; when SID is connected high, write address is 0x7A and read address is 0x7B.

note 4 when designing PCB, place chip power filter close to power pins; place 1μF capacitors near AVDD, DOVDD, DVDD, EVDD, VH, VN1, and VN2 in module; sensor's AGND and DGND should be separated inside module and outside PCB single-point connection; AVDD and AGND should not be adjacent to clock; power supply should be designed as thin as 0.12mm as much as possible and bottom line should be pulled to ground.

note 5 MCN/MCP, MDN0/MDP0, and MDN1/MDP1 are three pairs of differential lines; traces should be wrapped as long as possible.

2.3 format and frame

The OS02H10 supports RAW RGB output with a 2-lane MIPI interface.

table 2-1 MIPI formats and frame rates

format	resolution	max frame rate	methodology	10-bit output MIPI data rate	12-bit output MIPI data rate
1080p	1920x1080	60 fps	full resolution qualified pixel (1920+8) x (1080+8)	840 Mbps/lane (2-lane)	1008 Mbps/lane (2-lane)
1080p	1920x1080	30 fps	full resolution qualified pixel (1920+8) x (1080+8)	804 Mbps (1-lane) 420 Mbps/lane (2-lane)	1008 Mbps (1-lane) 504 Mbps/lane (2-lane)
2x binning	960x540	120 fps	2x2 binning qualified pixel (960+4) x (540+4)	804 Mbps (1-lane) 420 Mbps/lane (2-lane)	1008 Mbps (1-lane) 504 Mbps/lane (2-lane)

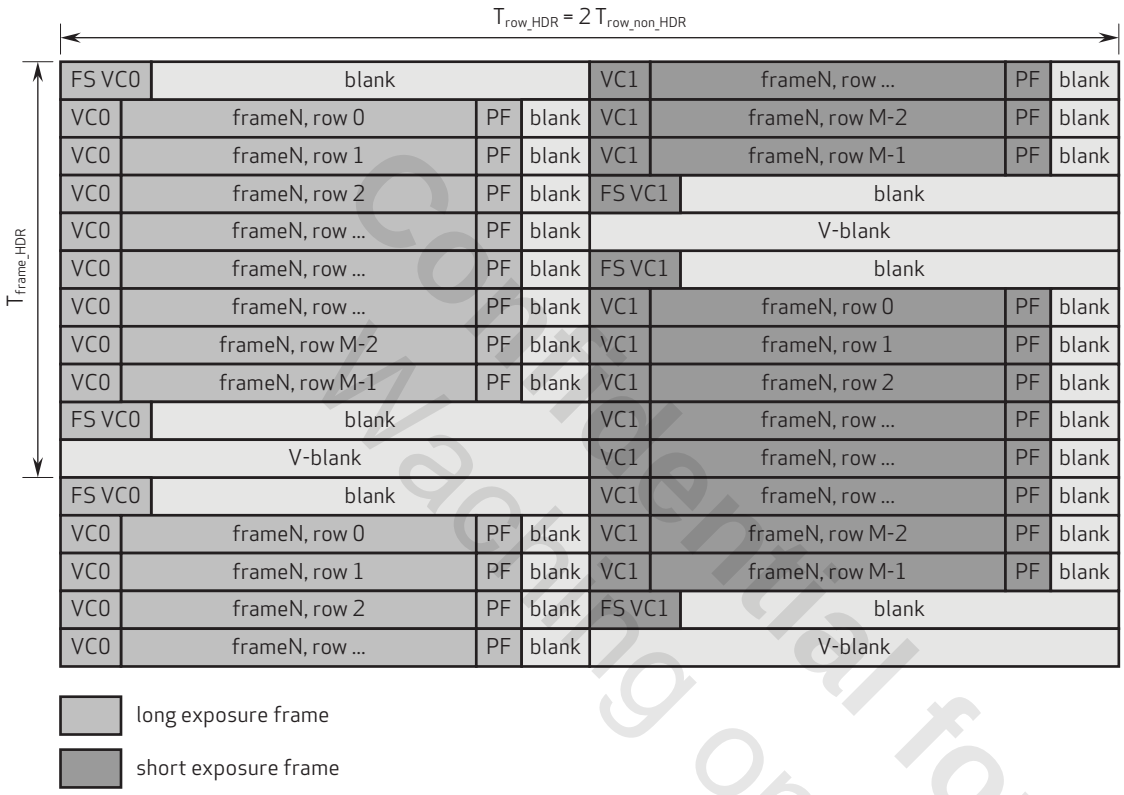
2.4 high dynamic range (HDR) mode

HDR mode increases image dynamic range by capturing two exposures of a similar scene and then combining them into one single image. The OS02H10 uses staggered HDR.

In staggered HDR mode, long/short exposure frames are overlapping with each other. This reduces the timing delay between different exposure frames, which will combine into one HDR frame. It also reduces the frame/line buffer needed for the backend chip.

In HDR mode, long and short frames are transmitted through virtual channels.

figure 2-3 long and short frame transmission in HDR mode



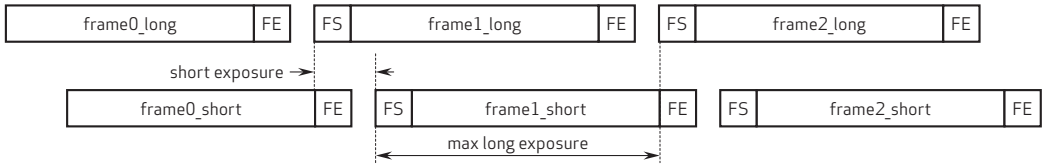
The OS02H10 supports two HDR modes:

- variable maximum short exposure HDR mode
- fixed maximum short exposure HDR mode

2.4.1 variable maximum short exposure HDR mode

The timing delay between long frame and short frame is short exposure.

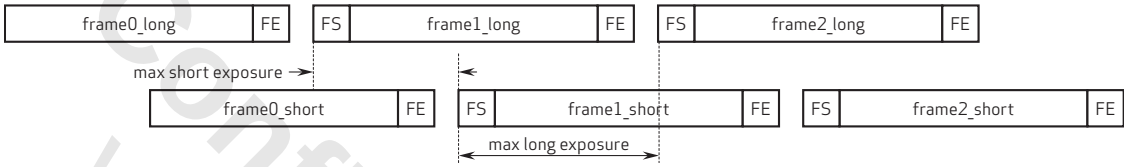
figure 2-4 variable maximum short exposure HDR mode



2.4.2 fixed maximum short exposure HDR mode

The timing delay between long frame and short frame is maximum short exposure and the maximum short exposure is set by registers.

figure 2-5 fixed maximum short exposure HDR mode



2.5 output interface

MIPI and LVDS data output interfaces are all integrated inside the OS02H10 sensor.

2.5.1 MIPI interface

The MIPI Interface is a serial interface, which can support high-speed, high-precision, and large-array transmissions. It plays an important role in security surveillance, video conferencing, traffic sign recognition, etc. With it, the OS02H10 can provide more high definition images to applications.

The MIPI inside the OS02H10 provides one single uni-directional clock lane and two data lane solutions for communication links between components inside the application device. This MIPI interface can support various operating modes, such as burst mode, switch mode, ULPS mode, and line sync mode. Users can select the appropriate mode according to their requirements.

2.5.2 D-PHY function

The D-PHY converts parallel data from CSI_TOP to serial data that is compatible with MIPI protocol. Detailed time sequences are shown in **figure 2-6** and **figure 2-7**.

figure 2-6 switching clock lane between clock transmission and low-power mode

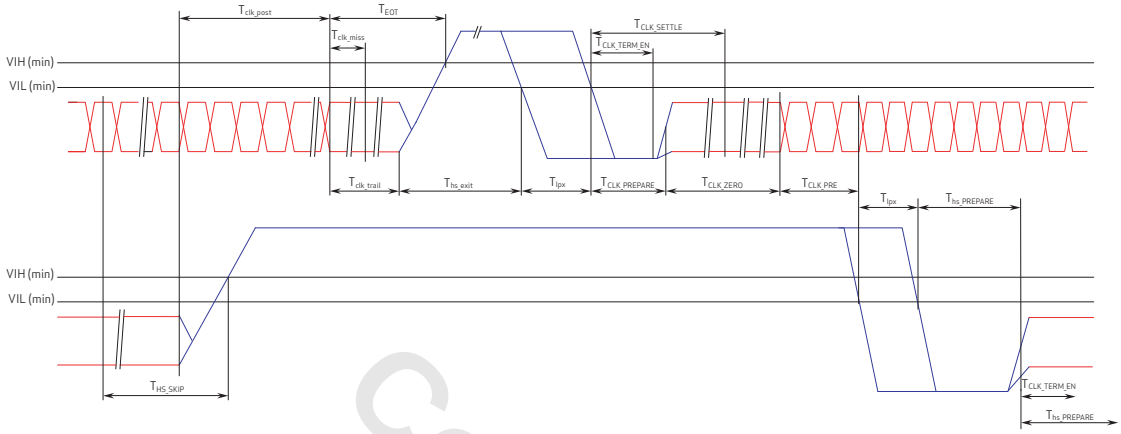
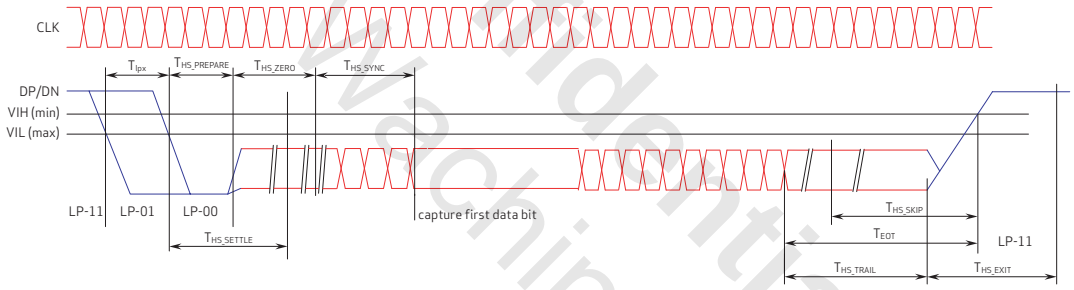


figure 2-7 high-speed data transmission bursts



2.5.3 data lane parameters

table 2-2 data lane parameters (sheet 1 of 2)

parameter	target	min	max
$T_{HS\text{-}PREPARE}$	time that transmitter drives data lane LP-00 line state immediately before HS-0 Line state starts HS transmission	40 ns + 4*UI	85 ns + 6*UI
$T_{HS\text{-}PREPARE}$ + $T_{HS\text{-}ZERO}$	$T_{HS\text{-}PREPARE}$ + time that transmitter drives HS-0 state prior to transmitting sync sequence	145 ns + 10*UI	
$T_{HS\text{-}SETTLE}$	time interval which HS receive shall ignore any data lane HS transitions, starting from beginning of $T_{HS\text{-}PREPARE}$	85 ns + 6*UI	145 ns + 10*UI

table 2-2 data lane parameters (sheet 2 of 2)

parameter	target	min	max
$T_{HS-SKIP}$	time interval which HS-RX should ignore any transitions on data lane, following a HS burst end point of interval is defined as beginning of LP-11 state following HS burst	40 ns	55 ns + 4*UI
$T_{HS-TRAIL}$	time that transmitter drives HS-0 state after last payload clock bit of a HS transmission burst	max (n*8*UI, 60 ns + n*4*UI)	
T_{LPX}	transmitted length of any low-power state period	50 ns	
T_{WAKEUP}	time that a transmitter drives a Mark-1 state prior to a stop state in order to initiate an exit from ULPS	1 ms	

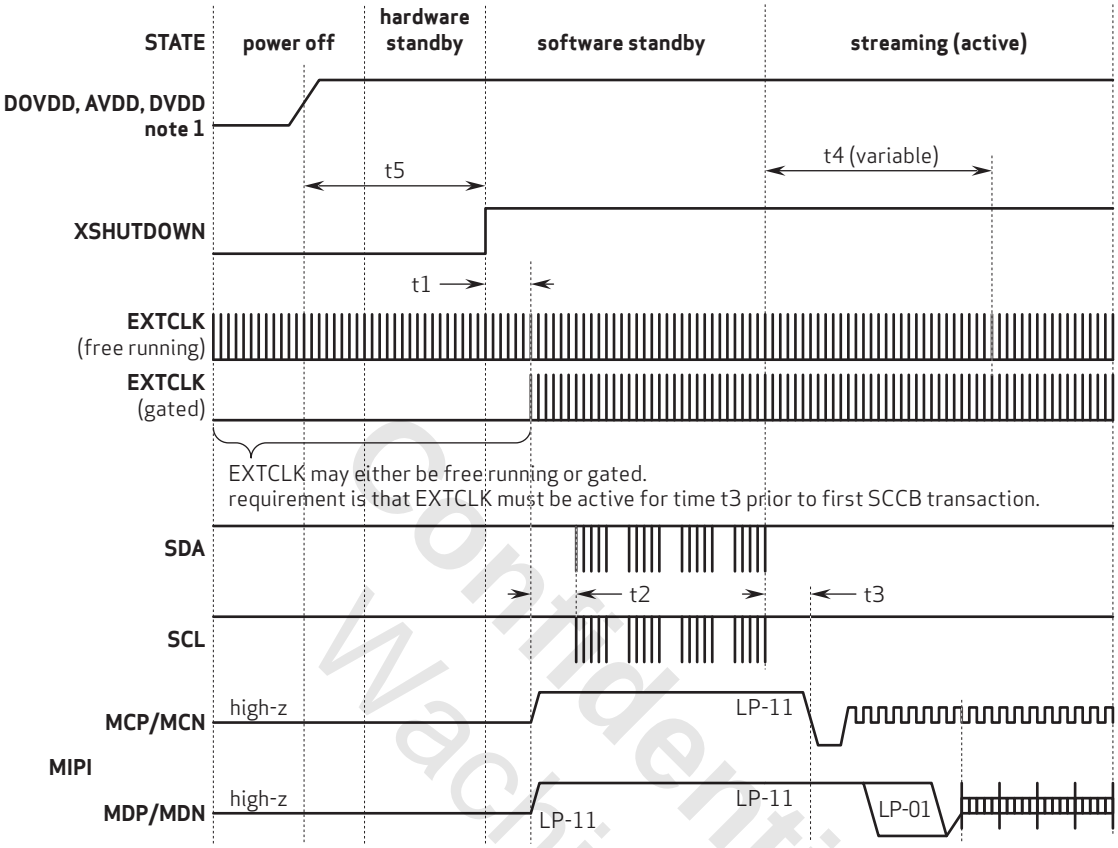
2.5.4 clock lane parameters

table 2-3 clock lane parameters

parameter	target	min	max
$T_{CLK-MISS}$	timeout for receiver to detect absence of clock transmission and disable clock lane HS-RX	60 ns	
$T_{CLK-POST}$	time that transmitter continues to send HS clock after last associated data lane has transitioned to LP mode, interval is defined as period from end of $T_{HS-TRAIL}$ to beginning $T_{CLK-TRAIL}$	60 ns + 52*UI	
$T_{CLK-PRE}$	time that HS clock will be driven by transmitter prior to any associated data lane beginning transition from LP to HS mode	8*UI	
$T_{CLK-PREPARE}$	time that transmitter drives clock lane LP-00 line state immediately before HS-0 line state starts HS transmission	38 ns	95 ns
$T_{CLK-SETTLE}$	time interval which HS receive will ignore any clock lane HS transmissions, starting from beginning of $T_{CLK-PREPARE}$	95 ns	300 ns
$T_{CLK-TRAIL}$	time that transmitter drives HS-0 state after last payload clock bit of a HS transmission burst	60 ns	
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that transmitter drives HS-0 state prior to starting clock	300 ns	
T_{EOT}	transmitted time interval from start of $T_{CLK-TRAIL}$ or $T_{HS-TRAIL}$, to start of LP-11 state following a HS burst		105 ns + n*12*UI

2.6 power up/off sequence

figure 2-8 power up sequence timing



note 1 DOVDD, AVDD and DVDD may rise in any order

table 2-4 power up sequence requirements

XSHUTDOWN	power up sequence requirements
GPIO	1. DOVDD, AVDD, and DVDD can rise in any order. 2. XSHUTDOWN rising must occur after AVDD, DOVDD and DVDD are stable.

table 2-5 power up sequence timing constraints

constraint	label	min	max	unit
XSHUTDOWN rising – system ready	t1	5		ms
minimum number of EXTCLK cycles prior to first SCCB transaction	t2	65535		EXTCLK cycles
MIPI clock startup time	t3		8192	EXTCLK cycles
entering streaming mode – first frame start sequence (variable)	t4	delay related to output frame rate and line timing		lines
AVDD, DOVDD or DVDD, whichever is last – XSHUTDOWN rising	t5	0	∞	ns

figure 2-9 power down sequence timing

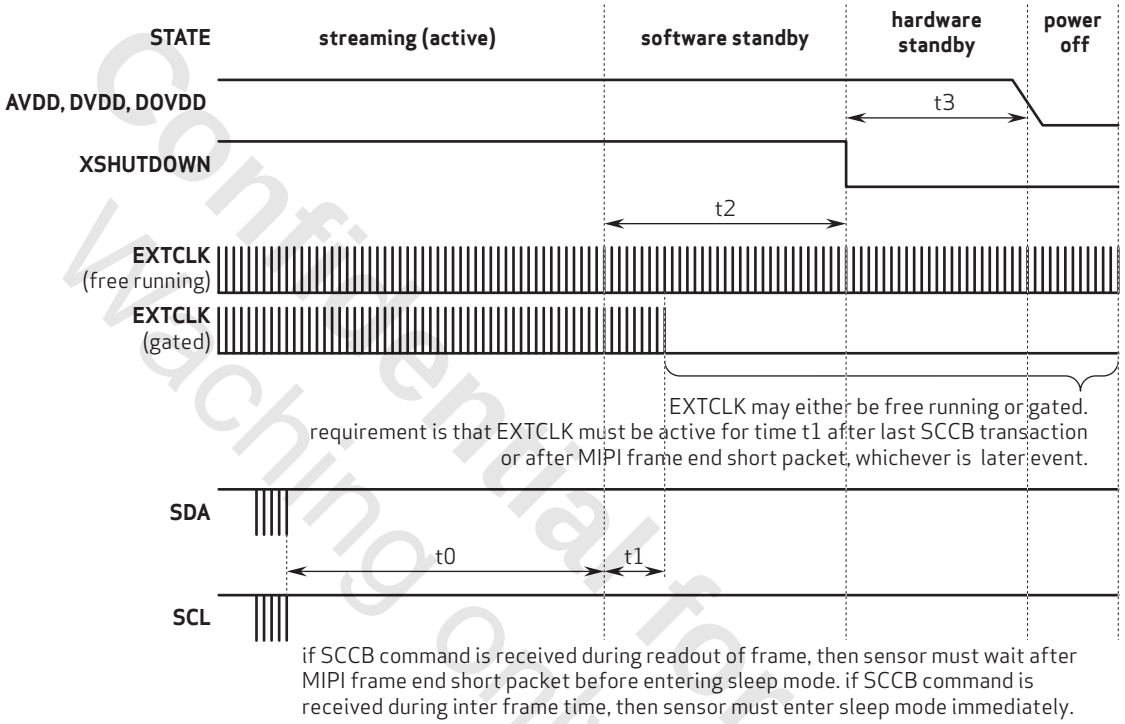


table 2-6 power down sequence requirements

XSHUTDOWN	power down sequence requirement
GPIO	1. Software standby recommended. 2. Pull XSHUTDOWN low for minimum power consumption. 3. Pull AVDD, DVDD, and DOVDD low in any order.

table 2-7 power down sequence timing constraints

constraint	label	min	max	unit
enter software standby SCCB command, device in software standby mode	t0	when a frame of MIPI data is output, wait for MIPI end code before entering software for standby; otherwise, enter software standby mode immediately		
minimum of EXTCLK cycles after last SCCB transaction or MIPI frame end	t1	512		EXTCLK cycles
last SCCB transaction or MIPI frame end, XSHUTDOWN falling	t2	512		EXTCLK cycles
XSHUTDOWN falling – AVDD, DVDD or DOVDD falling whichever is first	t3	0.0		ns

2.7 SCCB bus

2.7.1 single read and single write

The OS02H10 SCCB write address and read address can be selected by the SID pin. When the pin is set high, the write address is 0x7A and the read address is 0x7B. When the pin is set low, the write address is 0x78 and the read address is 0x79.

A typical read or write sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a '0' indicates a write and a '1' indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First, the master sends the write-mode slave address and 8-bit register address similar to the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The data transfer is stopped when the master sends a no-acknowledge bit.

figure 2-10 illustrates the OS02H10 single read sequence and single write sequence.

figure 2-10 SCCB read and write message description (SID pin set high)

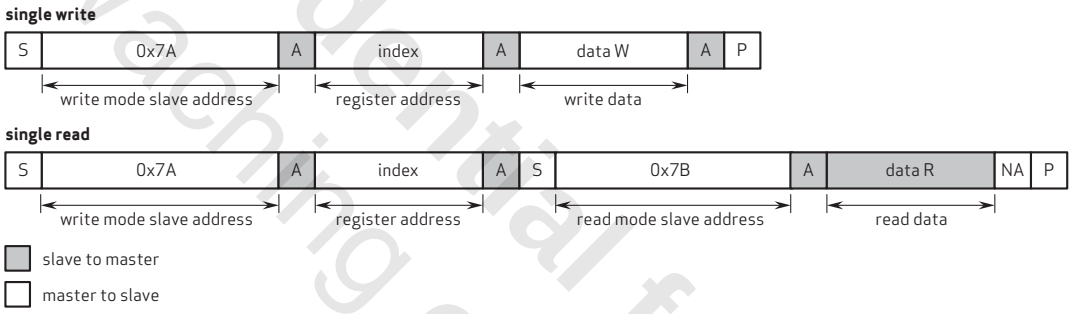
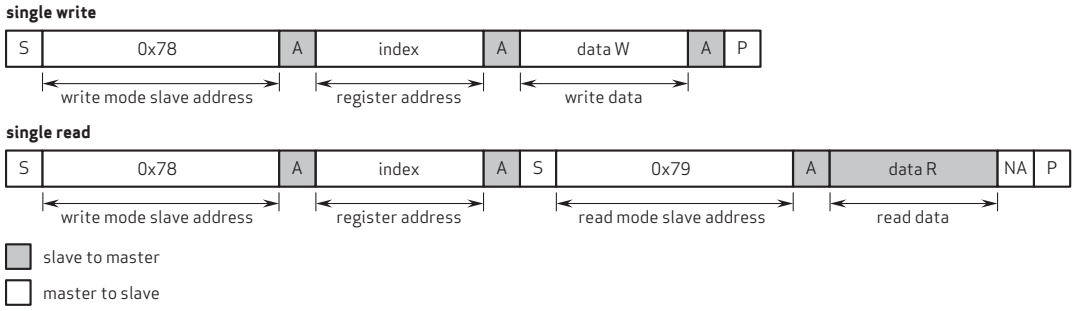


figure 2-11 SCCB read and write message description (SID pin set low)



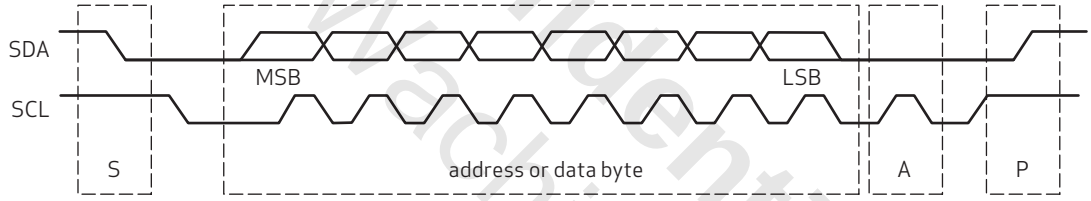
2.7.2 data bit transfer

One data bit is transferred during each clock pulse. The serial clock pulse is provided by the master. The data must be stable during the high period of the serial clock. It can only change when the serial clock is low. Data is transferred 8 bits at a time, followed by an acknowledge bit.

2.7.3 acknowledge bit

The OS02H10 will hold the value of the SDA pin to logic '0' during the logic '1' state of the acknowledge clock pulse on SCL.

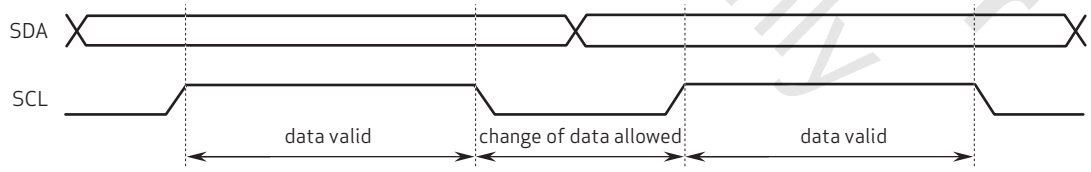
figure 2-12 SCCB acknowledge bit diagram



2.7.4 data valid

The master must ensure that the data is stable during the logic 1 state of the SCL pin. All transitions on the SDA pin can only occur when the logic level on the SCL pin is '0'.

figure 2-13 SCCB data transport diagram



2.7.5 timing parameter

figure 2-14 SCCB bus timing parameter diagram

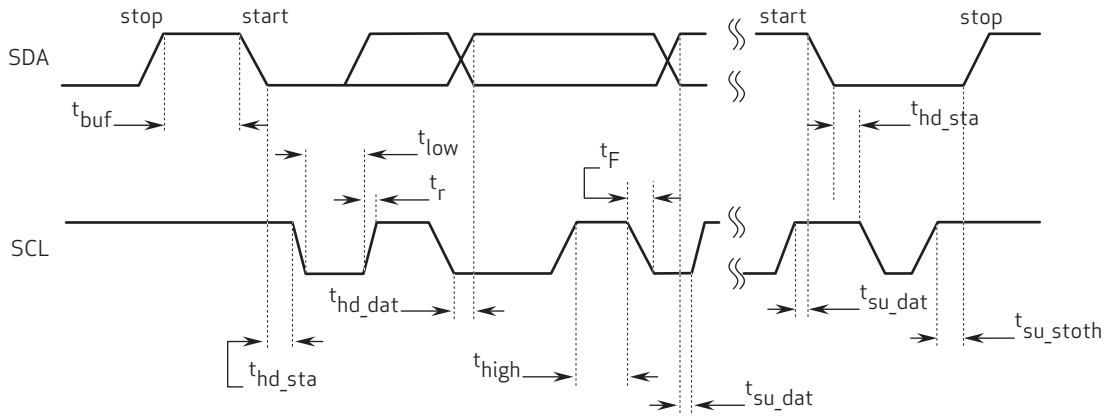


table 2-8 SCCB interface timing specifications

symbol	parameter	min	max	unit
f_{scl}	SCL clock frequency	–	400	kHz
t_{buf}	bus free time between a stop and a start	1.3	–	µs
t_{hd_sta}	hold time for a repeated start	0.6	–	µs
t_{low}	low period of SCL	1.3	–	µs
t_{high}	high period of SCL	0.6	–	µs
t_{su_sta}	setup time for a repeated start	0.6	–	µs
t_{hd_dat}	data hold time	0	–	µs
t_{su_dat}	data setup time	0.1	–	µs
t_r	rise time of SCL, SDA	–	0.3	µs
t_f	fall time of SCL, SDA	–	0.1	µs
t_{su_sto}	setup time for a stop	0.6	–	µs
t_{aa}	SCL low to data out valid	0.3	–	µs
t_{dh}	data out hold time	0.2	–	µs
C_b	capacitive load of bus line (SCL, SDA)	–	–	pf

3 block level description

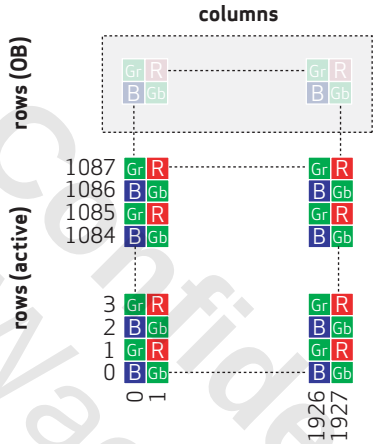
3.1 pixel array structure

The OS02H10 pixel array is configured as of 1928 columns by 1088 rows. The details of pixel array are shown in **figure 3-1**.

The color filters are arranged in a Bayer pattern. The primary color GR/BG array is arranged in line-alternating fashion.

The sensor array design is based on a field integration readout system with line-by-line transfer and an electronic shutter with a synchronous pixel readout scheme

figure 3-1 pixel array region color filter layout



3.2 binning

The OS02H10 supports a binning mode to provide a lower resolution output while maintaining field of view. With binning mode on, the voltage levels of adjacent pixels (of the same color) are averaged before being sent to the ADC. The OS02H10 supports vertical 1x2 color binning and horizontal 1x2 color binning, which is illustrated in **figure 3-2**, where the voltage levels of two horizontal (2x1) adjacent same-color pixels are averaged.

figure 3-2 example of horizontal 1x2 binning

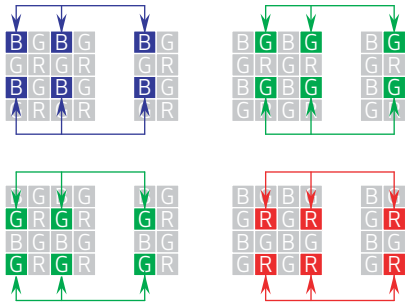


figure 3-3 example of vertical 1x2 binning

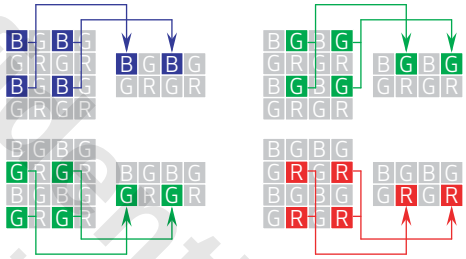
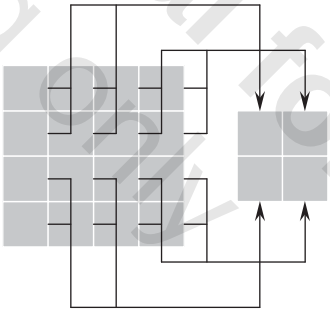


figure 3-4 example of 2x2 mono binning



3.3 10-bit A/D converters

The balanced signal is then digitized by the on-chip 10-bit ADC.

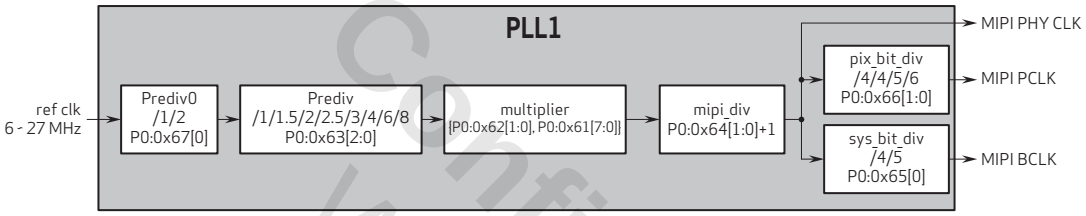
3.4 PLL and clock generator

The OS02H10 implements two PLLs with both inputs connected to the EXTCLK pin. One can support the MIPI bit clock, output clock PCLK, and internal BCLK, while the other one can support internal CNTCLK. In MIPI mode, the two PLLs can be used to optimize for EMC and/or minimize the required MIPI frequency.

3.4.1 PLL1

The PLL1 generates a default 168 MHz pixel clock (PCLK) and 840 MHz MIPI serial clock from a 6~27 MHz input clock. The VCO range is from 500 MHz to 1500 MHz. A programmable clock divider is provided to generate different frequencies.

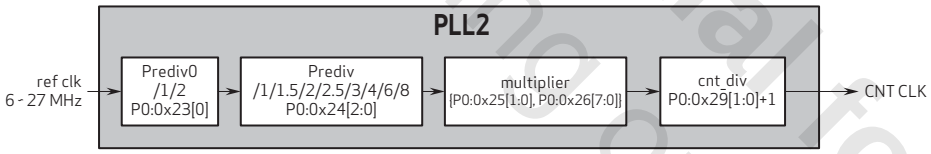
figure 3-5 PLL1 block diagram



3.4.2 PLL2

The PLL2 generates a default 360 MHz counter clock (CNTCLK) from a 6~27 MHz input clock. The VCO range is from 500 MHz to 1500 MHz. A programmable clock divider is provided to generate different frequencies.

figure 3-6 PLL2 block diagram



4 image sensor core digital functions

4.1 mirror and flip

The OS02H10 provides mirror and flip readout modes, which respectively reverse the sensor data readout order horizontally and vertically (see **figure 4-1**).

Mirror and flip are updated by exp_rpc_en (P1:0x01) register. It should be configured after configuring the mirror and flip register (P1:0x01 = 0x01).

figure 4-1 mirror and flip samples

original image | mirrored image | flipped image | mirrored and flipped image

table 4-1 mirror and flip registers

address	register name	default value	R/W	description
P1:0x3F	FLIP/MIRROR	0x00	RW	Bit[1:0]: Vertical flip/horizontal mirror 00: Normal (no flip) 01: Horizontal mirror 10: Vertical flip 11: Both horizontal mirror and vertical flip

4.2 windowing

4.2.1 digital windowing

The embedded windowing function extracts an image windowing area by defining four parameters, including horizontal start, horizontal width, vertical start, and vertical height (see **figure 4-2**). By properly setting the parameters, the portions within the sensor array size can be cropped as a visible area. The windowing function will not conflict with the mirror and flip functions.

figure 4-2 digital windowing diagram

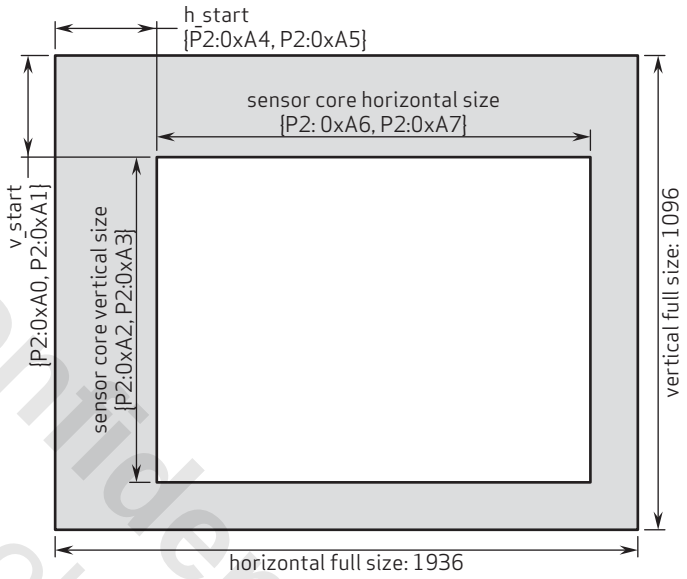


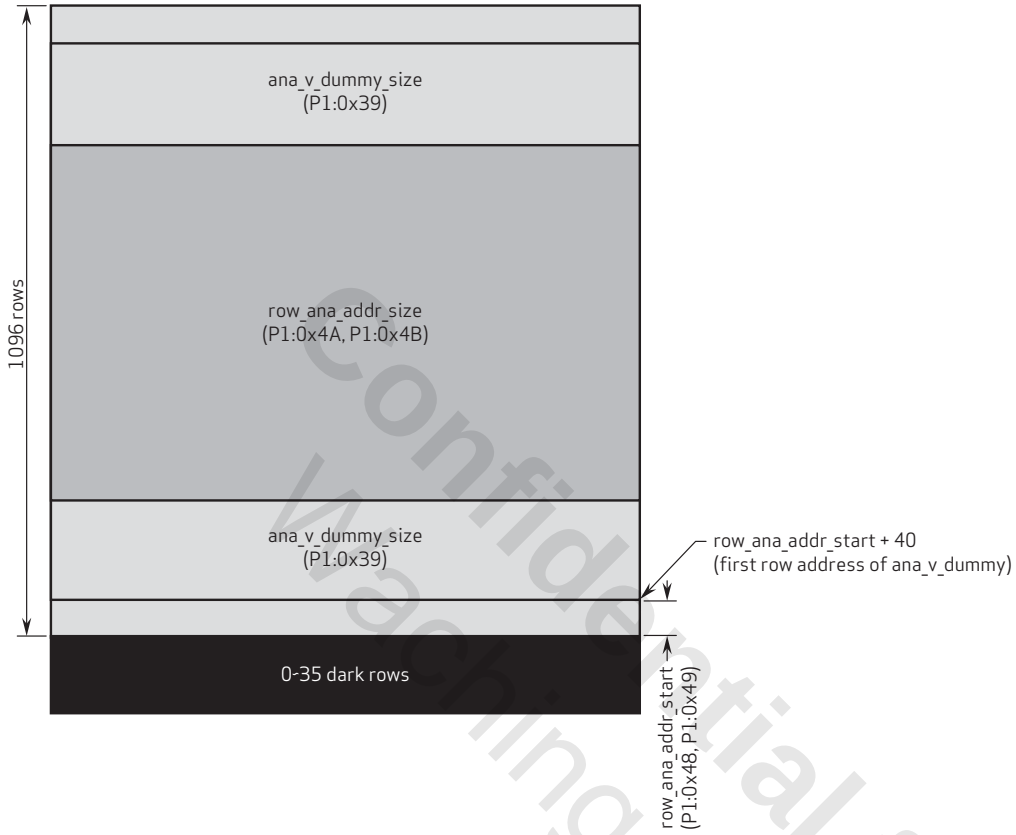
table 4-2 digital windowing control registers

address	register name	default value	R/W	description
P2:0xA0	DEM_V_START_3MSB	0x00	RW	Bit[2:0]: Image vertical start[10:8]
P2:0xA1	DEM_V_START_8LSB	0x00	RW	Bit[7:0]: Image vertical start[7:0]
P2:0xA2	DEM_V_SIZE_3MSB	0x04	RW	Bit[2:0]: Image vertical size[10:8]
P2:0xA3	DEM_V_SIZE_8LSB	0x48	RW	Bit[7:0]: Image vertical size[7:0]
P2:0xA4	DEM_H_START_3MSB	0x00	RW	Bit[2:0]: Image horizontal start[10:8]
P2:0xA5	DEM_H_START_8LSB	0x00	RW	Bit[7:0]: Image horizontal start[7:0]
P2:0xA6	DEM_H_SIZE_3MSB	0x07	RW	Bit[2:0]: Image horizontal size[10:8]
P2:0xA7	DEM_H_SIZE_8LSB	0x90	RW	Bit[7:0]: Image horizontal size[7:0]

4.2.2 analog windowing

The embedded analog windowing function extracts an image windowing area by defining four parameters, including horizontal start, horizontal width, vertical start, and vertical height. By properly setting the parameters, the portions within the sensor array size can be cropped as a visible area. The analog windowing function can increase frame rate and the window area will not be affected by mirror or flip function.

figure 4-3 full size mode

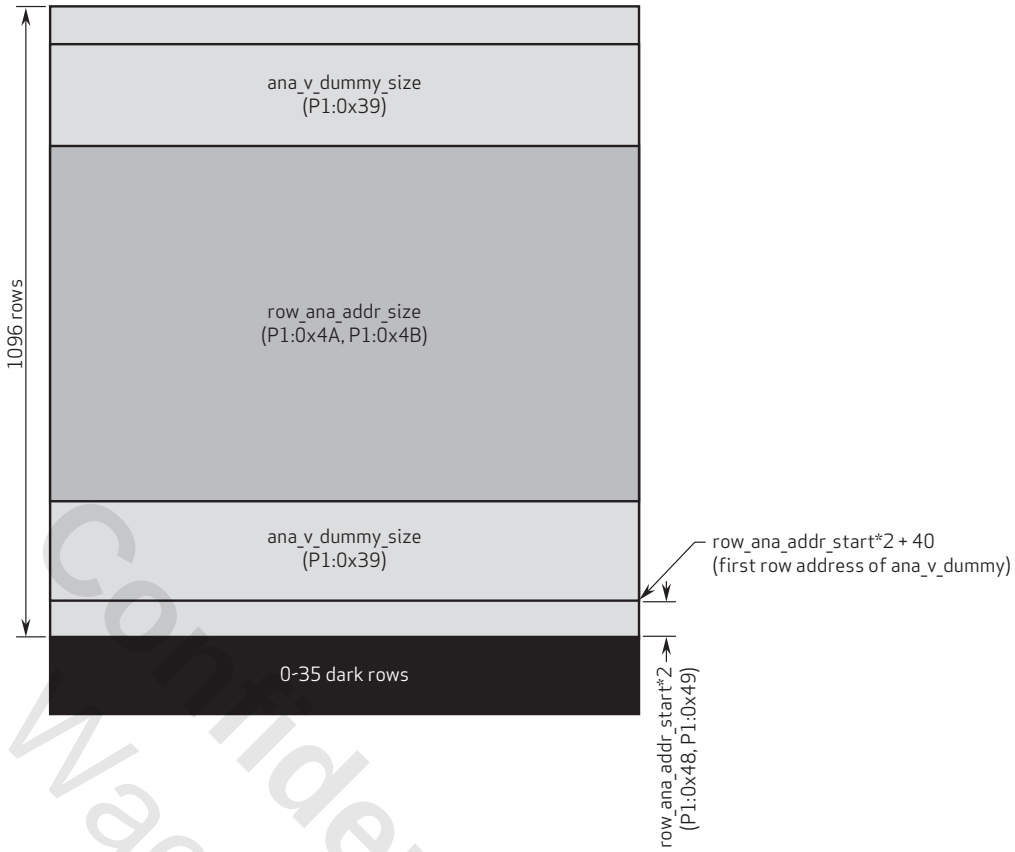


In the ana_window mode, output row number is row_ana_addr_size + ana_v_dummy_size * 2. Do not output rows (except dark rows) and do not reset and read.

row_ana_addr_start is the spacing between the window's first row to dark rows:
row_ana_addr_start = (1936 - row_ana_addr_size - ana_v_dummy_size * 2)/2.

Note: row_ana_addr_size, ana_v_dummy_size, and row_ana_addr_start must be an even number.

figure 4-4 binning mode



In the binning ana_window mode, output row number is (row_ana_addr_size + ana_v_dummy_size * 2)/2; do not output rows (except dark rows) and do not reset/read.

row_ana_addr_start is the spacing between the window's first row to dark rows:
row_ana_addr_start = (548 - (row_ana_addr_size + ana_v_dummy_size * 2)/2)/2; output column number is col_ana_addr_size; col_ana_addr_start is the column start of window; for windows in the middle of a full size image:
col_ana_addr_start = (1936 - col_ana_addr_size)/2

table 4-3 analog windowing control registers

address	register name	default value	R/W	description
P1:0x39	ANA_V_DUMMY_SIZE	0x10	RW	Bit[7:0]: ana_v_dummy_size Specify vertical row number upward and downward of active readout area, respectively, for analog window mode
P1:0x3A	COL_ANA_ADDR_START_2MSB	0x00	RW	Bit[1:0]: col_ana_addr_start[9:8]
P1:0x3B	COL_ANA_ADDR_START_8LSB	0x00	RW	Bit[7:0]: col_ana_addr_start[7:0]
P1:0x3C	COL_ANA_ADDR_SIZE_2MSB	0x03	RW	Bit[1:0]: col_ana_addr_size[9:8]
P1:0x3D	COL_ANA_ADDR_SIZE_8LSB	0x3C	RW	Bit[7:0]: col_ana_addr_size[7:0]
P1:0x48	ROW_ANA_ADDR_START_3MSB	0x00	RW	Bit[2:0]: row_ana_addr_start[10:8]
P1:0x49	ROW_ANA_ADDR_START_8LSB	0x00	RW	Bit[7:0]: row_ana_addr_start[7:0]
P1:0x4A	ROW_ANA_ADDR_SIZE_3MSB	0x02	RW	Bit[2:0]: row_ana_addr_size[10:8]
P1:0x4B	ROW_ANA_ADDR_SIZE_8LSB	0xD8	RW	Bit[7:0]: row_ana_addr_size[7:0]

4.3 test pattern

Test pattern and color bar are offered for testing purposes.

figure 4-5 test pattern diagram

table 4-4 test enable register

address	register name	default value	R/W	description
P1:0x0D	TEST_EN	1'b0	RW	Bit[0]: test_en 0: Disable color bar 1: Enable color bar

4.4 auto black level calibration (BLC)

The BLC function is used to set the pixel out of a complete black object to a programmable pedestal value in all kinds of lightning conditions. Due to circuit offset and pixel dark current, the pixel output level of a black object is normally non-zero. The OS02H10 calibrates the black level of the active pixel by subtracting the true optical black pixel output.

The BLC is based on measuring the value at the center of the distribution of the optical black reference pixels and applying digital correction to bring the center to the target value. The center of the pixel distribution is estimated from a combination of median and average filtering. The filtering for the BLC is based on the middle 1024 columns of 16 optical dark rows. Only the values closest to the horizontal center of each row are used in order to minimize influence from any edge effects in the array.

During normal operation, dark current is expected to change slowly with time. During slow changes, the BLC in the OS02H10 will use multi frame iterative averaging statistics for a more stable change. The frame number can be set by the register P2:0x6D[2:1].

table 4-5 auto BLC registers (sheet 1 of 5)

address	register name	default value	R/W	description
P2:0x64	TPM_DATA_MAX_8MSB	0x10	RW	Bit[7:0]: tpm_data_max[15:8]
P2:0x65	TPM_DATA_MAX_8LSB	0x00	RW	Bit[7:0]: tpm_data_max[7:0]
P2:0x66	DC_LEVEL_LIMIT_DATA_8LSB	0x20	RW	Bit[7:0]: Limitation of DC[7:0]
P2:0x67	DC_LEVEL_LIMIT_DATA_2MSB	0x03	RW	Bit[1:0]: Limitation of DC[9:8]
P2:0x68	RANDOM_SEL, ADC_HIGH_8BIT, DC_LEVEL_LIMIT_EN	0x02	RW	Bit[2]: random_sel Bit[1]: adc_high_8bit Bit[0]: dc_level_limit_en
P2:0x69	BLC_LIMIT_DATA_8LSB	0xE8	RW	Bit[7:0]: Limitation of data output[7:0]
P2:0x6A	BLC_LIMIT_DATA_2MSB	0x03	RW	Bit[1:0]: Limitation of data output[9:8]
P2:0x6B	KSCG_EN, CIS_DATA_CLAMP_EN, CIS_DATA_RAND_EN	0x00	RW	Bit[2]: kscg_en Bit[1]: cis_data_clamp_en Bit[0]: cis_data_rand_en

table 4-5 auto BLC registers (sheet 2 of 5)

address	register name	default value	R/W	description
P2:0x6D	ABL	0x00	RW	Bit[7]: blc_test_en 0: Low 10-bit output mode 1: High 10-bit output mode Bit[6]: blc_filter_en 0: Dark row median filter disable 1: Dark row median filter enable Bit[5]: ob2_en 0: OB2 disable 1: OB2 enable Bit[4]: blc_bpc_en 0: Dark row BPC disable 1: Dark row BPC enable Bit[3]: random_en 0: Add random value disable 1: Add random value enable Bit[2:1]: blc_mode 00: 1 frame average mode 01: 4 frames average mode 10: 8 frames average mode 11: 1 frame average mode Bit[0]: blc_en 0: Black level disable 1: Black level enable
P2:0x6E	ABL_TRIGGER	0x00	RW	Bit[7]: scg_en_trigger Bit[6]: tpm_trigger Bit[5]: Auto BLC enable Bit[4]: Gain trigger Bit[3]: Exposure trigger Bit[2]: mean_trigger Bit[1]: Refresh BLC sum Bit[0]: Manual trigger
P2:0x6F	TRIG_FRAMECOUNT	0x02	RW	Bit[3]: trig_framecount
P2:0x70	BLC_DATA_SEL, BL_POSITION_SET2, BL_POSITION_SET	0x00	RW	Bit[4]: blc_data_sel Bit[3:2]: bl_position_set2 Bit[1:0]: bl_position_set
P2:0x71	BL_POSITION1_SET2, BL_POSITION1_SET	0x00	RW	Bit[3:2]: bl_position1_set2 Bit[1:0]: bl_position1_set
P2:0x72	BLUE_SUBOFFSET_8LSB	0x00	RW	Bit[7:0]: Black level offset, blue channel[7:0] Total register is 9 bits with MSB at P2:0x76[7]

table 4-5 auto BLC registers (sheet 3 of 5)

address	register name	default value	R/W	description
P2:0x73	RED_SUBOFFSET_8LSB	0x00	RW	Bit[7:0]: Black level offset, red channel[7:0] Total register is 9 bits with MSB at P2:0x76[6]
P2:0x74	GR_SUBOFFSET_8LSB	0x00	RW	Bit[7:0]: Black level offset, Gr channel[7:0] Total register is 9 bits with MSB at P2:0x76[5]
P2:0x75	GB_SUBOFFSET_8LSB	0x00	RW	Bit[7:0]: Black level offset, Gb channel[7:0] Total register is 9 bits with MSB at P2:0x76[4]
P2:0x76	BLUE_SUBOFFSET_1MSB, RED_SUBOFFSET_1MSB, GR_SUBOFFSET_1MSB, GB_SUBOFFSET_1MSB	0x00	RW	Bit[7]: Black level offset, blue channel[8] High 1 bit, which is sign bit, and low bits are at P2:0x72[7:0] Bit[6]: Black level offset, red channel[8] High 1 bit, which is sign bit, and low bits are at P2:0x73[7:0] Bit[5]: Black level offset, Gr channel[8] High 1 bit, which is sign bit, and low bits are at P2:0x74[7:0] Bit[4]: Black level offset, Gb channel[8] High 1 bit, which is sign bit, and low bits are at P2:0x75[7:0]
P2:0x77	BLC_CHANNEL_SEL	0x07	RW	Bit[2:0]: blc_channel_sel
P2:0x78	BLC_EXP_BLUE	0x80	RW	Bit[7:0]: blc_exp_blue[7:0]
P2:0x79	BLC_EXP_RED	0x80	RW	Bit[7:0]: blc_exp_red[7:0]
P2:0x7A	BLC_EXP_GR	0x80	RW	Bit[7:0]: blc_exp_gr[7:0]
P2:0x7B	BLC_EXP_GB	0x80	RW	Bit[7:0]: blc_exp_gb[7:0]
P2:0x7C	BLC_RPC_BLUE	0x00	RW	Bit[5:0]: blc_rpc_blue
P2:0x7D	BLC_RPC_RED	0x00	RW	Bit[5:0]: blc_rpc_red
P2:0x7E	BLC_RPC_GR	0x00	RW	Bit[5:0]: blc_rpc_gr
P2:0x7F	BLC_RPC_GB	0x00	RW	Bit[5:0]: blc_rpc_gb
P2:0x80	BLC_BPC_TH_P_8LSB	0x40	RW	Bit[7:0]: blc_bpc_th_p[7:0] Black level positive threshold for bad pixels, encoded in absolute value

table 4-5 auto BLC registers (sheet 4 of 5)

address	register name	default value	R/W	description
P2:0x81	BLC_BPC_TH_N_8LSB	0xC0	RW	Bit[7:0]: blc_bpc_th_n[7:0] Black level negative threshold for bad pixels, encoded in absolute value
P2:0x82	BLC_MEAN_MAX	0x00	RW	Bit[7:0]: Black level shift, blue channel 0x00~0xFF: 0~255
P2:0x83	BLC_BPC_IN_P_8LSB	0xC0	RW	Bit[7:0]: blc_bpc_in_p[7:0] Black level positive threshold for bad pixels, encoded in absolute value
P2:0x84	BLC_BPC_IN_N_8LSB	0xC0	RW	Bit[7:0]: blc_bpc_in_n[7:0] Black level negative threshold for bad pixels, encoded in absolute value
P2:0x85	GAIN_LIMIT	0x0C	RW	Bit[5:0]: Black level shift Gb channel 0x00~0xFF: 0~255
P2:0x86	BLACK_LEVEL_GB_8LSB	–	R	Bit[7:0]: black_level_gb[7:0]
P2:0x87	BLACK_LEVEL_B_8LSB	–	R	Bit[7:0]: black_level_b[7:0]
P2:0x88	BLACK_LEVEL_R_8LSB	–	R	Bit[7:0]: black_level_r[7:0]
P2:0x89	BLACK_LEVEL_GR_8LSB	–	R	Bit[7:0]: black_level_gr[7:0]
P2:0x8A	BLACK_LEVEL_GB_8MSB	–	R	Bit[7:0]: black_level_gb[15:8]
P2:0x8B	BLACK_LEVEL_B_8MSB	–	R	Bit[7:0]: black_level_b[15:8]
P2:0x8C	BLACK_LEVEL_R_8MSB	–	R	Bit[7:0]: black_level_r[15:8]
P2:0x8D	BLACK_LEVEL_GR_8MSB	–	R	Bit[7:0]: black_level_gr[15:8]
P2:0x8E	BLACK1_LEVEL_GB_8LSB	–	R	Bit[7:0]: black1_level_gb[7:0]
P2:0x8F	BLACK1_LEVEL_B_8LSB	–	R	Bit[7:0]: black1_level_b[7:0]
P2:0x90	BLACK1_LEVEL_R_8LSB	–	R	Bit[7:0]: black1_level_r[7:0]
P2:0x91	BLACK1_LEVEL_GR_8LSB	–	R	Bit[7:0]: black1_level_gr[7:0]
P2:0x92	BLACK1_LEVEL_GB_8MSB	–	R	Bit[7:0]: black1_level_gb[15:8]
P2:0x93	BLACK1_LEVEL_B_8MSB	–	R	Bit[7:0]: black1_level_b[15:8]
P2:0x94	BLACK1_LEVEL_R_8MSB	–	R	Bit[7:0]: black1_level_r[15:8]
P2:0x95	BLACK1_LEVEL_GR_8MSB	–	R	Bit[7:0]: black1_level_gr[15:8]
P2:0x97	BLC_EXP_BLUE1	0x80	RW	Bit[7:0]: blc_exp_blue1[7:0]
P2:0x98	BLC_EXP_RED1	0x80	RW	Bit[7:0]: blc_exp_red1[7:0]

table 4-5 auto BLC registers (sheet 5 of 5)

address	register name	default value	R/W	description
P2:0x99	BLC_EXP_GR1	0x80	RW	Bit[7:0]: blc_exp_gr1[7:0]
P2:0x9A	BLC_EXP_GB1	0x80	RW	Bit[7:0]: blc_exp_gb1[7:0]
P2:0x9B	BLC_RPC_BLUE1	0x00	RW	Bit[5:0]: blc_rpc_blue1
P2:0x9C	BLC_RPC_RED1	0x00	RW	Bit[5:0]: blc_rpc_red1
P2:0x9D	BLC_RPC_GR1	0x00	RW	Bit[5:0]: blc_rpc_gr1
P2:0x9E	BLC_RPC_GB1	0x00	RW	Bit[5:0]: blc_rpc_gb1
P2:0x9F	BLC_MEAN_MAX1	0x00	RW	Bit[7:0]: blc_mean_max1

4.5 OTP defect pixel correction

Defect pixels will be detected and replaced by a value calculated from the neighboring pixel during the bad pixel correction (BPC) unit.

A defect pixel, which is black and is not charged when light hits it, is a pixel with a zero value when it is read. Such bad pixels will be detected and corrected.

In defect pixel processing, according to the exposure time and the analog gain, a pixel will be divided into four states (outdoor, normal, dummy, and lowlight). Different BPC thresholds can be used in different states.

Module enable priority (from top to bottom):

- P2:0x52[3]: OTP BPC module (demo_gf) bypass enable
- P2:0x60[3:0]: OTP BPC enable
- P2:0x52[0]: OTP sends double defect pixels coordinates enable

table 4-6 OTP defect pixel correction registers (sheet 1 of 2)

address	register name	default value	R/W	description
P2:0x60	LSC_BPC_EN	0x0F	RW	Bit[3]: OTP bpc_short enable in outdoor Bit[2]: OTP bpc_short enable in lowlight Bit[1]: OTP BPC enable in outdoor Bit[0]: OTP BPC enable in lowlight
P2:0x62	ROW_START_8LSB	0x01	RW	Bit[7:0]: row_start[7:0] BPC start row number low 8 bits
P2:0x63	ROW_START_3MSB	0x00	RW	Bit[2:0]: row_start[10:8] BPC start row number high 3 bits
P4:0x12	ISP_REGF_12	0x10	RW	Bit[7:0]: bpc_dif_thr_outdoor BPC grad difference threshold in outdoor in long frame

table 4-6 OTP defect pixel correction registers (sheet 2 of 2)

address	register name	default value	R/W	description
P4:0x13	ISP_REGF_13	0x10	RW	Bit[7:0]: bpc_dif_thr_low BPC grad difference threshold in lowlight in long frame
P4:0x14	ISP_REGF_14	0x10	RW	Bit[7:0]: bpc_grad_thr_outdoor BPC edge grad threshold in outdoor in long frame
P4:0x15	ISP_REGF_15	0x10	RW	Bit[7:0]: bpc_grad_thr_low BPC edge grad threshold in lowlight in long frame
P4:0x33	ISP_REGF_33	0x10	RW	Bit[7:0]: bpc_dif_thr_outdoor BPC grad difference threshold in outdoor in short frame
P4:0x34	ISP_REGF_34	0x10	RW	Bit[7:0]: bpc_dif_thr_low BPC grad difference threshold in lowlight in short frame
P4:0x35	ISP_REGF_35	0x10	RW	Bit[7:0]: bpc_grad_thr_outdoor BPC edge grad threshold in outdoor in short frame
P4:0x36	ISP_REGF_36	0x10	RW	Bit[7:0]: bpc_grad_thr_low BPC edge grad threshold in lowlight in short frame

table 4-7 dynamic defect pixel correction registers (sheet 1 of 3)

address	register name	default value	R/W	description
P2:0x00	ISP_CTRL_1_L	0x1B	RW	Bit[7]: Enable tail Bit[6]: Enable general tail Enable tailing cluster Bit[5]: Enable 3x3 cluster Bit[4]: Enable saturate cross cluster Bit[3]: Enable cross cluster Bit[2]: Manual mode enable Bit[1]: Black pixel enable Bit[0]: White pixel enable
P2:0x01	ISP_CTRL_1	0x94	RW	Bit[7:6]: Vertical number list[2] Bit[5:4]: Vertical number list[1] Bit[3:2]: Vertical number list[0] Bit[1]: Clip interpG Enable G clip Bit[0]: Enable share buffer No connect

table 4-7 dynamic defect pixel correction registers (sheet 2 of 3)

address	register name	default value	R/W	description
P2:0x02	ISP_CTRL_2	0x2E	RW	Bit[5:4]: Bayer pattern order Bit[3:2]: Edge option Image boundary extend options Bit[1:0]: Vertical number list[3]
P2:0x03	ISP_CTRL_3	0x24	RW	Bit[6:3]: White pixel threshold list[0] Bit[2:0]: Maximum vertical number
P2:0x04	ISP_CTRL_4	0x12	RW	Bit[7:4]: White pixel threshold list[2] Bit[3:0]: White pixel threshold list[1]
P2:0x05	ISP_CTRL_5	0x41	RW	Bit[7:4]: BThresRatio Dark pixel threshold ratio Bit[3:0]: White pixel threshold list[3]
P2:0x06	ISP_CTRL_6	0x48	RW	Bit[7:4]: Status threshold Bit[3:0]: MoreConnectionCaseThre Cluster threshold
P2:0x07	ISP_CTRL_7	0x84	RW	Bit[7:4]: MatchingThre Pattern match threshold Bit[3:0]: Status threshold step
P2:0x08	ISP_CTRL_8	0x40	RW	Bit[7:4]: Adaptive pattern step Bit[3:0]: Adaptive pattern threshold
P2:0x09	ISP_CTRL_9	0x00	RW	Bit[3:0]: Saturate pixel threshold for clusters
P2:0x0A	ISP_CTRL_10	0x00	RW	Bit[4:0]: Gain threshold list[0][4:0]
P2:0x0B	ISP_CTRL_11	0x00	RW	Bit[4:0]: Gain threshold list[1][4:0]
P2:0x0C	ISP_CTRL_12	0x01	RW	Bit[4:0]: Gain threshold list[2][4:0]
P2:0x0D	ISP_CTRL_13	0x0F	RW	Bit[7:0]: DPC level list[0]
P2:0x0E	ISP_CTRL_14	0xFD	RW	Bit[7:0]: DPC level list[1]
P2:0x0F	ISP_CTRL_15	0xF5	RW	Bit[7:0]: DPC level list[2]
P2:0x10	ISP_CTRL_16	0xF5	RW	Bit[7:0]: DPC level list[3]
P2:0x14	ISP_CTRL_20	0x00	RW	Bit[7:5]: Recover clock gate disable Bit[4]: SRAM clock gate disable Bit[3]: Buffer control clock gate disable Bit[2]: Start frame clock gate disable Bit[1]: Clock gate disable Bit[0]: Pixel order manual enable
P2:0x18	ISP_CTRL_24	–	R	Bit[6:0]: Bthre
P2:0x19	ISP_CTRL_25	–	R	Bit[4:0]: Wthre Wthre_list
P2:0x1A	ISP_CTRL_26	–	R	Bit[4:0]: Thre1 matching_thre
P2:0x1B	ISP_CTRL_27	–	R	Bit[7:0]: Thre2 status_thre

table 4-7 dynamic defect pixel correction registers (sheet 3 of 3)

address	register name	default value	R/W	description
P2:0x1C	ISP_CTRL_28	–	R	Bit[6:0]: Thre3adptive_pattern_thre
P2:0x1D	ISP_CTRL_29	–	R	Bit[6:0]: Thre4more_conn_case_thre
P2:0x1E	ISP_CTRL_30	–	R	Bit[7:4]: Level Bit[3:0]: Pconnected
P2:0x1F	ISP_CTRL_31	–	R	Bit[2:0]: Vnum
P2:0x20	ISP_CTRL_1_S	0x1B	RW	Bit[7]: Enable tail Bit[6]: Enable general tail Enable tailing cluster Bit[5]: Enable 3x3 cluster Bit[4]: Enable saturate cross cluster Bit[3]: Enable cross cluster Bit[2]: Manual mode enable Bit[1]: Black pixel enable Bit[0]: White pixel enable
P2:0x40	CFA_PTN, CEN_GLOBAL, SCLK_GT_DIS	0x12	RW	Bit[5:4]: cfa_ptn Bit[1]: cen_global Bit[0]: sclk_gt_dis
P2:0x43	HSIZE_DPC_3MSB	0x07	RW	Bit[2:0]: hsize_dpc[10:8]
P2:0x44	HSIZE_DPC_8LSB	0x88	RW	Bit[7:0]: hsize_dpc[7:0]
P2:0x45	GAINLIST_0_L_4LSB, GAINLIST_1_L_4LSB	0x3F	RW	Bit[7:4]: Gain threshold list_l[0][3:0] Bit[3:0]: Gain threshold list_l[1][3:0]
P2:0x46	GAINLIST_2_L_4LSB, GAINLIST_2_S_4LSB	0xFF	RW	Bit[7:4]: Gain threshold list_l[2][3:0] Bit[3:0]: Gain threshold list_s[2][3:0]
P2:0x47	GAINLIST_0_S_4LSB, GAINLIST_1_S_4LSB	0x3F	RW	Bit[7:4]: Gain threshold list_s[0][3:0] Bit[3:0]: Gain threshold list_s[1][3:0]
P2:0x52	ISP_MODE	0xFE	RW	Bit[7]: dpc_s_en Dynamic DPC enable in short frame 0: Disable 1: Enable Bit[4]: dpc_l_en Dynamic DPC enable in long frame 0: Disable 1: Enable Bit[3]: demo_en demo_gf power down enable 0: Enable demo_gf power down 1: Disable demo_gf power down Bit[0]: dp_pos_en 0: Disable 1: Enable read OTP DPC data

4.6 digital gain/analog gain

Channel digital gain can be controlled by DG_Gr, DG_Gb, DG_R, and DG_B. Each digital gain can be configured from a gain of 0 to 2.

Global digital gain can be controlled from a gain of 1 to 32.

Analog gain can be obtained by adjusting the ramp's slope register (pga_gain_ctl). Analog gain can be configured from a gain of 1 to 32. Analog gain is updated by register of exp_rpc_en (P1:0x01). It should be configured after configuring the analog gain register (P1:0x01 = 0x01).

table 4-8 digital gain/analog gain registers

address	register name	default value	R/W	description
P1:0x24	PGA_GAIN1_CTL	0x20	RW	Bit[7:0]: pga_gain1[7:0] Long frame RPC gain low byte pga_gain1 = {P1:0x3E[0], P1:0x24[7:0]} 0x000~0x1FF: 1x~31x
P1:0x3E	SIG_GAIN1_EN, GAIN_2X_SEL, SCG_EN_SHORT, SCG_EN_LONG, PGA_GAIN2_1MSB, PGA_GAIN1_1MSB	0x10	RW	Bit[5]: sig_gain1_en Bit[4]: gain_2x_sel Bit[3]: scg_en_short Bit[2]: scg_en_long Bit[1]: pga_gain2[8] Short frame RPC gain high bit Bit[0]: pga_gain1[8] Long frame RPC gain high bit
P1:0x45	PGA_GAIN2_CTL	0x20	RW	Bit[7:0]: pga_gain2[7:0] Short frame RPC gain low byte pga_gain2 = {P1:0x3E[1], P1:0x45[7:0]} 0x000~0x1FF: 1x~31x

table 4-9 register mapping relationship

configuration gain RPC[8:4]	mapping gain pga_gain_ctl
5'h01	{3'h0, RPC[3:0]}
5'h02, 5'h03	{3'h1, RPC[4:1]}
5'h04, 5'h05, 5'h06, 5'h07	{3'h2, RPC[5:2]}
5'h08, 5'h09, 5'h0A, 5'h0B, 5'h0C, 5'h0D, 5'h0E, 5'h0F	{3'h3, RPC[6:3]}
5'h10, 5'h11, 5'h12, 5'h13, 5'h14, 5'h15, 5'h16, 5'h17, 5'h18, 5'h19, 5'h1A, 5'h1B, 5'h1C, 5'h1D, 5'h1E, 5'h1F	{3'h4, RPC[7:4]}

table 4-10 actual analog gain (sheet 1 of 3)

code (hex)	gain code bit[6]	gain code bit[5]	gain code bit[4]	gain code bit[3]	gain code bit[2]	gain code bit[1]	gain code bit[0]	gain
0x00	0	0	0	0	0	0	0	1*(1+0/16)
0x01	0	0	0	0	0	0	1	1*(1+1/16)
0x02	0	0	0	0	0	1	0	1*(1+2/16)
0x03	0	0	0	0	0	1	1	1*(1+3/16)
0x04	0	0	0	0	1	0	0	1*(1+4/16)
0x05	0	0	0	0	1	0	1	1*(1+5/16)
0x06	0	0	0	0	1	1	0	1*(1+6/16)
0x07	0	0	0	0	1	1	1	1*(1+7/16)
0x08	0	0	0	1	0	0	0	1*(1+8/16)
0x09	0	0	0	1	0	0	1	1*(1+9/16)
0x0A	0	0	0	1	0	1	0	1*(1+10/16)
0x0B	0	0	0	1	0	1	1	1*(1+11/16)
0x0C	0	0	0	1	1	0	0	1*(1+12/16)
0x0D	0	0	0	1	1	0	1	1*(1+13/16)
0x0E	0	0	0	1	1	1	0	1*(1+14/16)
0x0F	0	0	0	1	1	1	1	1*(1+15/16)
0x10	0	0	1	0	0	0	0	2*(1+0/16)
0x11	0	0	1	0	0	0	1	2*(1+1/16)
0x12	0	0	1	0	0	1	0	2*(1+2/16)
0x13	0	0	1	0	0	1	1	2*(1+3/16)
0x14	0	0	1	0	1	0	0	2*(1+4/16)
0x15	0	0	1	0	1	0	1	2*(1+5/16)
0x16	0	0	1	0	1	1	0	2*(1+6/16)
0x17	0	0	1	0	1	1	1	2*(1+7/16)
0x18	0	0	1	1	0	0	0	2*(1+8/16)
0x19	0	0	1	1	0	0	1	2*(1+9/16)
0x1A	0	0	1	1	0	1	0	2*(1+10/16)
0x1B	0	0	1	1	0	1	1	2*(1+11/16)
0x1C	0	0	1	1	1	0	0	2*(1+12/16)

table 4-10 actual analog gain (sheet 2 of 3)

code (hex)	gain code bit[6]	gain code bit[5]	gain code bit[4]	gain code bit[3]	gain code bit[2]	gain code bit[1]	gain code bit[0]	gain
0x1D	0	0	1	1	1	0	1	2*(1+13/16)
0x1E	0	0	1	1	1	1	0	2*(1+14/16)
0x1F	0	0	1	1	1	1	1	2*(1+15/16)
0x20	0	1	0	0	0	0	0	4*(1+0/16)
0x21	0	1	0	0	0	0	1	4*(1+1/16)
0x22	0	1	0	0	0	1	0	4*(1+2/16)
0x23	0	1	0	0	0	1	1	4*(1+3/16)
0x24	0	1	0	0	1	0	0	4*(1+4/16)
0x25	0	1	0	0	1	0	1	4*(1+5/16)
0x26	0	1	0	0	1	1	0	4*(1+6/16)
0x27	0	1	0	0	1	1	1	4*(1+7/16)
0x28	0	1	0	1	0	0	0	4*(1+8/16)
0x29	0	1	0	1	0	0	1	4*(1+9/16)
0x2A	0	1	0	1	0	1	0	4*(1+10/16)
0x2B	0	1	0	1	0	1	1	4*(1+11/16)
0x2C	0	1	0	1	1	0	0	4*(1+12/16)
0x2D	0	1	0	1	1	0	1	4*(1+13/16)
0x2E	0	1	0	1	1	1	0	4*(1+14/16)
0x2F	0	1	0	1	1	1	1	4*(1+15/16)
0x30	0	1	1	0	0	0	0	8*(1+0/16)
0x31	0	1	1	0	0	0	1	8*(1+1/16)
0x32	0	1	1	0	0	1	0	8*(1+2/16)
0x33	0	1	1	0	0	1	1	8*(1+3/16)
0x34	0	1	1	0	1	0	0	8*(1+4/16)
0x35	0	1	1	0	1	0	1	8*(1+5/16)
0x36	0	1	1	0	1	1	0	8*(1+6/16)
0x37	0	1	1	0	1	1	1	8*(1+7/16)
0x38	0	1	1	1	0	0	0	8*(1+8/16)
0x39	0	1	1	1	0	0	1	8*(1+9/16)

table 4-10 actual analog gain (sheet 3 of 3)

code (hex)	gain code bit[6]	gain code bit[5]	gain code bit[4]	gain code bit[3]	gain code bit[2]	gain code bit[1]	gain code bit[0]	gain
0x3A	0	1	1	1	0	1	0	8*(1+10/16)
0x3B	0	1	1	1	0	1	1	8*(1+11/16)
0x3C	0	1	1	1	1	0	0	8*(1+12/16)
0x3D	0	1	1	1	1	0	1	8*(1+13/16)
0x3E	0	1	1	1	1	1	0	8*(1+14/16)
0x3F	0	1	1	1	1	1	1	8*(1+15/16)
0x40	1	0	0	0	0	0	0	16*(1+0/16)
0x41	1	0	0	0	0	0	1	16*(1+1/16)
0x42	1	0	0	0	0	1	0	16*(1+2/16)
0x43	1	0	0	0	0	1	1	16*(1+3/16)
0x44	1	0	0	0	1	0	0	16*(1+4/16)
0x45	1	0	0	0	1	0	1	16*(1+5/16)
0x46	1	0	0	0	1	1	0	16*(1+6/16)
0x47	1	0	0	0	1	1	1	16*(1+7/16)
0x48	1	0	0	1	0	0	0	16*(1+8/16)
0x49	1	0	0	1	0	0	1	16*(1+9/16)
0x4A	1	0	0	1	0	1	0	16*(1+10/16)
0x4B	1	0	0	1	0	1	1	16*(1+11/16)
0x4C	1	0	0	1	1	0	0	16*(1+12/16)
0x4D	1	0	0	1	1	0	1	16*(1+13/16)
0x4E	1	0	0	1	1	1	0	16*(1+14/16)
0x4F	1	0	0	1	1	1	1	16*(1+15/16)

4.7 exposure control

The OS02H10 exposure time can be set manually by registers:

- minimum exposure is one line
- {P1:0x03[7:0], P1:0x04[7:0]} for exposure time

All exposure time values are represented by unit of row time: row time = HTS / row clock

It can adjust the line time through the Hblank register ({P1:0x09, P1:0x0A}), where row clock is the system clock and HTS is the horizontal total size that can be read by registers {P1:0xDA, P1:0xDB}.

It can adjust the line time through the Vblank register ({P1:0x05, P1:0x06}), where the frame rate is adjusted after confirmed resolution.

The length of the frame can be determined by reading the register frame_length_readonly ({P1:0x4E, P1:0x4F}).

In full size (v_sub mode), frame length is the readout value of frame_length_readonly ({P1:0x4E, P1:0x4F}).

In binning and VGA mode, the actual frame length is double the read value of frame_length_readonly ({P1:0x4E, P1:0x4F}).

Exposure time/Vblank/Hblank is updated by register of exp_rpc_en (P1:0x01). It is should be configured after configuring the exposure time/Vblank/Hblank register (P1:0x01 = 0x01).

table 4-11 exposure control registers (sheet 1 of 2)

address	register name	default value	R/W	description
P1:0x03	BUF_EXP_8MSB	0x01	RW	Bit[7:0]: buf_exp[15:8] Exposure time high byte in "H" unit 0x0001~0xFFFF: 1~65535
P1:0x04	BUF_EXP_8LSB	0x9A	RW	Bit[7:0]: buf_exp[7:0] Exposure time low byte in "H" unit 0x0001~0xFFFF: 1~65535
P1:0x05	VBLANK_BUF_8MSB	0x00	RW	Bit[7:0]: vblank_buf[15:8] Vertical blank high byte in "H" unit 0x0001~0xFFFF: 1~65535
P1:0x06	VBLANK_BUF_8LSB	0x00	RW	Bit[7:0]: vblank_buf[7:0] Vertical blank low byte in "H" unit 0x0001~0xFFFF: 1~65535
P1:0x08	VPOS_BLANK	0x01	RW	Bit[3:0]: vpos_blank Time width between posedge of VSYNC and posedge of first HSYNC in "H" unit

table 4-11 exposure control registers (sheet 2 of 2)

address	register name	default value	R/W	description
P1:0x09	HBLANK_4MSB	0x00	RW	Bit[3:0]: Hblank[11:8] Horizontal blank high byte in "timer_clk" unit 0x000~0xFFF: 0~4095
P1:0x0A	HBLANK_8LSB	0x00	RW	Bit[7:0]: Hblank[7:0] Horizontal blank low byte in "timer_clk" unit 0x000~0xFFF: 0~4095
P1:0x41	VDELAY_BUF_8MSB	0x00	RW	Bit[7:0]: vdelay_buf[15:8] Vertical blank when exposure is greater than frame length high byte in "H" unit
P1:0x42	VDELAY_BUF_8LSB	0x00	RW	Bit[7:0]: vdelay_buf[7:0] Vertical blank when exposure is greater than frame length low byte in "H" unit
P1:0xDA	HTS_8MSB	–	R	Bit[7:0]: HTS[15:8] Horizontal total size high byte
P1:0xDB	HTS_8LSB	–	R	Bit[7:0]: HTS[7:0] Horizontal total size low byte

4.8 one-time programmable (OTP) memory

The OS02H10 has a total of 256 bytes of OTP memory. When using the auto load function, the data in the OTP memory is written to registers when the sensor is powered up (e.g., DPC data).

5 register tables

5.1 system control [P0:0x02 - P0:0x05, P0:0x1B - P0:0x71]

table 5-1 system control registers (sheet 1 of 5)

address	register name	default value	R/W	description
P0:0x02	CHIP_ID	0x53	R	Bit[7:0]: chip_id[31:24]
P0:0x03	CHIP_ID	0x02	R	Bit[7:0]: chip_id[23:16]
P0:0x04	CHIP_ID	0x48	R	Bit[7:0]: chip_id[15:8]
P0:0x05	CHIP_ID	0x10	R	Bit[7:0]: chip_id[7:0]
P0:0x1B	IE_FSIN, VSYNC_OUT_EN_BUF, STROBE_OUT_EN_BUF	0x07	RW	Bit[7:3]: Not used Bit[2]: ie_fsin Bit[1]: vsync_out_en_buf Bit[0]: strobe_out_en_buf
P0:0x1C~ P0:0x1D	RSVD	–	–	Reserved
P0:0x1E	DS_FSIN, DS_VSYNC, DS_STROBE	0x15	RW	Bit[7:6]: Not used Bit[5:4]: ds_fsin Bit[3:2]: ds_vsync Bit[1:0]: ds_strobe
P0:0x1F	RSVD	–	–	Reserved
P0:0x20	MODE_SEL_EN_BUF, SOFT_RST	0x01	RW	Bit[7:5]: Not used Bit[4]: mode_sel_en_buf Bit[3:1]: Not used Bit[0]: soft_rst
P0:0x21	PLL_R_CP_BUF	0x00	RW	Bit[7:2]: Not used Bit[1:0]: pll_r_cp_buf
P0:0x22	PLL_BP_BUF, PLL_DIV_RST_BUF, PLL_RST_BUF	0x00	RW	Bit[7:3]: Not used Bit[2]: pll_bp_buf Bit[1]: pll_div_rst_buf Bit[0]: pll_rst_buf
P0:0x23	PLL_R_PREDIVP_BUF	0x00	RW	Bit[7:1]: Not used Bit[0]: pll_r_predivp_buf
P0:0x24	PLL_R_PREDIV_BUF	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pll_r_prediv_buf
P0:0x25	PLL_R_DIVP_2MSB_BUF	0x00	RW	Bit[7:2]: Not used Bit[1:0]: pll_r_divp_buf[9:8]
P0:0x26	PLL_R_DIVP_8LSB_BUF	0x3C	RW	Bit[7:0]: pll_r_divp_buf[7:0]

table 5-1 system control registers (sheet 2 of 5)

address	register name	default value	R/W	description
P0:0x27	PLL_R_DIV_RST_SYNC_EN _BUF	0x00	RW	Bit[7:1]: Not used Bit[0]: pll_r_div_rst_sync_en_buf
P0:0x28	PLL_R_DIVS_BUF	0x00	RW	Bit[7:2]: Not used Bit[1:0]: pll_r_divs_buf
P0:0x29	PLL_R_DIVDAC_BUF	0x00	RW	Bit[7:2]: Not used Bit[1:0]: pll_r_divdac_buf
P0:0x2A	PLL_R_DIVSRAM_BUF	0x03	RW	Bit[7:3]: Not used Bit[2:0]: pll_r_divsram_buf
P0:0x2B	PLL_R_BAND_SEL_BUF	0x00	RW	Bit[7:1]: Not used Bit[0]: pll_r_band_sel_buf
P0:0x2C	PLL_R_VCOBY2_BUF	0x01	RW	Bit[7:1]: Not used Bit[0]: pll_r_vcoby2_buf
P0:0x2D	PLL_R_EN_EXTI_BUF	0x00	RW	Bit[7:1]: Not used Bit[0]: pll_r_en_exti_buf
P0:0x2E~ P0:0x30	RSVD	–	–	Reserved
P0:0x31	CLK_MODE_BUF	0x90	RW	Bit[7]: pll_clk_ctrl 0: pll_clk = pclk_in 1: pll_clk = pclk_in/2 Bit[6:4]: row_clk_mode 000: row_clk = timer_clk (or clk) 001: row_clk = timer_clk (or clk)/2 010: row_clk = timer_clk (or clk)/4 100: row_clk = timer_clk (or clk)/8 Others: Not defined Bit[3]: Not used Bit[2:0]: timer_clk_ctrl 000: timer_clk = pll_pclk 001: timer_clk = pll_pclk/2 010: timer_clk = pll_pclk/4 100: timer_clk = pll_pclk/8 Others: Not defined

table 5-1 system control registers (sheet 3 of 5)

address	register name	default value	R/W	description
P0:0x32	CLK_MODE2_BUF	0x04	RW	Bit[7:5]: Not used Bit[4]: row_clk_cel 0: row_clk from timer_clk 1: row_clk from clkin Bit[3:2]: bclk_ctrl 00: mipi_bclk_phy = mipi_bclkin 01: mipi_bclk_phy = mipi_bclkin/2 10: mipi_bclk_phy = mipi_bclkin/4 11: Not defined Bit[1:0]: dclk_ctrl 00: dclk = timer_clk 01: dclk = timer_clk/2 10: dclk = timer_clk/4 11: Not defined
P0:0x33~ P0:0x36	RSVD	–	–	Reserved
P0:0x37	PWD_ASP	0x00	RW	Bit[7:1]: Not used Bit[0]: pwd_asp
P0:0x38	LVDS_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: lvds_en
P0:0x39~ P0:0x3F	RSVD	–	–	Reserved
P0:0x40	EXT_SYNC_MST_EN, EXT_SYNC_EN	–	RW	Bit[7:2]: Not used Bit[1]: ext_sync_mst_en Enable master mode of external sync function 0: OS02H10 is slave of external sync 1: OS02H10 is master of external sync Bit[0]: ext_sync_en Enable signal of external sync function 0: Disable external sync 1: Enable external sync
P0:0x41~ P0:0x4F	RSVD	–	–	Reserved
P0:0x50	SCCB_DEV_ADDR_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: sccb_dev_addr_en
P0:0x51	SCCB_DEV_ADDR	0x3D	RW	Bit[7]: Not used Bit[6:0]: sccb_dev_addr

table 5-1 system control registers (sheet 4 of 5)

address	register name	default value	R/W	description
P0:0x52	OSC_CLK_DIV_GATING_BUF, PLL_CLK_OSC_GATING_BUF	0x19	RW	Bit[7:5]: Not used Bit[4]: osc_clk_div_gating_buf Bit[3]: pll_clk_osc_gating_buf Bit[2:0]: Not used
P0:0x53	SCCB_MEM_GATING_BUF, OTP_GATING_BUF, TPM_CLK_GATING_BUF, TEST_PATTERN_GATING_BUF, BLC_GATING_BUF, DPC_GATING_BUF, OTP_DPC_GATING_BUF, LVDS_GATING_BUF	0x9F	RW	Bit[7]: sccb_mem_gating_buf Bit[6]: otp_gating_buf Bit[5]: tpm_clk_gating_buf Bit[4]: test_pattern_gating_buf Bit[3]: blc_gating_buf Bit[2]: dpc_gating_buf Bit[1]: otp_dpc_gating_buf Bit[0]: lvds_gating_buf
P0:0x54	DPC_VBL_GATING_BUF, MIPI_PCLK_INV_EN_BUF, OB_GATING_BUF, COL_CLK_GATING_EN_BUF, EXT_SYNC_GATING_BUF, STROBE_GATING_BUF, MIPI_GATING_BUF, BCLK_GATING_BUF	0x3F	RW	Bit[7]: dpc_vbl_gating_buf Bit[6]: mipi_pclk_inv_en_buf Bit[5]: ob_gating_buf Bit[4]: col_clk_gating_en_buf Bit[3]: ext_sync_gating_buf Bit[2]: strobe_gating_buf Bit[1]: mipi_gating_buf Bit[0]: bclk_gating_buf
P0:0x55	PCLK_IN_SEL_BUF	0x00	RW	Bit[7:1]: Not used Bit[0]: pclk_in_sel_buf
P0:0x56	SCCB_MEM_STANDBY, SCCB_BIST_ERROR, SCCB_BIST_DONE, SCCB_BIST_EN	0x00	RW	Bit[7:5]: Not used Bit[4]: sccb_mem_standby Bit[3]: Not used Bit[2]: sccb_bist_error (read only) Bit[1]: sccb_bist_done (read only) Bit[0]: sccb_bist_en
P0:0x57~ P0:0x5F	RSVD	–	–	Reserved
P0:0x60	MPLL_CP_BUF	0x01	RW	Bit[7:3]: Not used Bit[2:0]: mpll_cp
P0:0x61	MPLL_DIVP_8LSB_BUF	0x8C	RW	Bit[7:0]: mpll_divp[7:0]
P0:0x62	MPLL_DIVP_2MSB_BUF	0x00	RW	Bit[7:2]: Not used Bit[1:0]: mpll_divp[9:8]
P0:0x63	MPLL_PREDIV_BUF	0x05	RW	Bit[7:3]: Not used Bit[2:0]: mpll_prediv
P0:0x64	MPLL_DIVOUT_BUF	0x02	RW	Bit[7:2]: Not used Bit[1:0]: mpll_divout
P0:0x65	MPLL_DIVSYS_BUF	0x00	RW	Bit[7:1]: Not used Bit[0]: mpll_divsys

table 5-1 system control registers (sheet 5 of 5)

address	register name	default value	R/W	description
P0:0x66	MPLL_DIVBIT_BUF	0x02	RW	Bit[7:2]: Not used Bit[1:0]: mpll_divbit
P0:0x67	MPLL_PREDIVP_BUF	0x00	RW	Bit[7:1]: Not used Bit[0]: mpll_predivp
P0:0x68	MPLL_DIV_RST_SYNC_ EN_BUF	0x00	RW	Bit[7:1]: Not used Bit[0]: mpll_div_rst_sync_en
P0:0x69~ P0:0x6B	RSVD	–	–	Reserved
P0:0x6C	MPLL_RST_BUF	0x00	RW	Bit[7:1]: Not used Bit[0]: mpll_rst
P0:0x6D	MPLL_BP_BUF	0x00	RW	Bit[7:1]: Not used Bit[0]: mpll_bp
P0:0x6E	MPLL_DIV_RST_BUF	0x00	RW	Bit[7:1]: Not used Bit[0]: mpll_div_rst
P0:0x6F~ P0:0x71	RSVD	–	–	Reserved

5.2 MIPI control [P0:0x8D - P0:0xB6]

table 5-2 MIPI control registers (sheet 1 of 2)

address	register name	default value	R/W	description
P0:0x8D	MIPI_RST, MIPI_PD	0x03	RW	Bit[7:2]: Not used Bit[1]: mipi_rst Bit[0]: mipi_pd
P0:0x8E	HSIZE_MIPI_4MSB	0x07	RW	Bit[7:4]: Not used Bit[3:0]: hsize_mipi[11:8]
P0:0x8F	HSIZE_MIPI_8LSB	0x88	RW	Bit[7:0]: hsize_mipi[7:0]
P0:0x90	VSIZE_MIPI_3MSB	0x04	RW	Bit[7:3]: Not used Bit[2:0]: vsize_mipi[10:8]
P0:0x91	VSIZE_MIPI_8LSB	0x40	RW	Bit[7:0]: vsize_mipi[7:0]
P0:0x92	HS_MODE_VF, HS_MODE	0x02	RW	Bit[7:2]: Not used Bit[1]: hs_mode_vf Bit[0]: hs_mode
P0:0x93	R_CLK_POST	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: r_clk_post
P0:0x94	R_LPX_CK, R_LPX_DAT	0x77	RW	Bit[7:4]: r_lpx_ck Bit[3:0]: r_lpx_dat
P0:0x95	R_CK_PREPARE, R_DAT_PREPARE	0x56	RW	Bit[7:4]: r_ck_prepare Bit[3:0]: r_dat_prepare
P0:0x96	R_HS_ZERO	0x1A	RW	Bit[7:5]: Not used Bit[4:0]: r_hs_zero
P0:0x97	DATA_ID	0x2B	RW	Bit[7:0]: data_id for long frame
P0:0x98	R_CK_TRAIL, R_DAT_TRAIL	0x78	RW	Bit[7:4]: r_ck_trail Bit[3:0]: r_dat_trail
P0:0x99	DATA_ID_EMB	0x2B	RW	Bit[7:0]: data_id for emb line
P0:0x9A	DATA_ID1	0x12	RW	Bit[7:0]: data_id for short frame
P0:0x9B	STAGGER MODE	0x00	RW	Bit[7:1]: Not used Bit[0]: Stagger mode enable
P0:0x9C	R_CLK_ZERO	0x22	RW	Bit[7:6]: Not used Bit[5:0]: r_clk_zero
P0:0x9D~ P0:0xA0	RSVD	–	–	Reserved

table 5-2 MIPI control registers (sheet 2 of 2)

address	register name	default value	R/W	description
P0:0xA1	MIPI_LS_START_NUM, TX_SPEED_AREA_SEL	0x05	RW	Bit[7:5]: Not used Bit[4:3]: mipi_ls_start_num Bit[2:0]: tx_speed_area_sel 0x00~0x04: Auto 0x05: Manual
P0:0xA2	R_INIT_8MSB	0x0B	RW	Bit[7:0]: r_init[15:8]
P0:0xA3	R_INIT_8LSB	0x40	RW	Bit[7:0]: r_init[7:0]
P0:0xA4	R_EXIT, R_WAKEUP_MH	0x10	RW	Bit[7:6]: Not used Bit[5:3]: r_exit Bit[2]: Not used Bit[1:0]: r_wakeup[17:16]
P0:0xA5	R_WAKEUP_M	0x86	RW	Bit[7:0]: r_wakeup[15:8]
P0:0xA6	R_WAKEUP_L	0x88	RW	Bit[7:0]: r_wakeup[7:0]
P0:0xA7~ P0:0xB0	RSVD	–	–	Reserved
P0:0xB1	MIPI_EMB_EN, MIPI_EN	0x00	RW	Bit[7:2]: Not used Bit[1]: mipi_emb_en 0: Disable MIPI emb mode 1: Enable MIPI emb mode Bit[0]: MIPI enable 0: Disable MIPI 1: Enable MIPI
P0:0xB3	VIRTUAL CHANNEL	0x04	RW	Virtual Channel Bit[7:4]: Not used Bit[3:2]: Virtual channel for long frame Bit[1:0]: Virtual channel for short frame
P0:0xB4~ P0:0xB5	RSVD	–	–	Reserved
P0:0xB6	DOUBLE, PAULE_CK, LS_MODE, INIT, ULP_MODE, TEST_MODE	0x40	RW	Bit[7]: Not used Bit[6]: Double Bit[5]: paule_ck Bit[4]: ls_mode Bit[3]: Init Bit[2]: ulp_mode Bit[1:0]: test_mode

5.3 TMS [P0:0xB7]

table 5-3 TMS register

address	register name	default value	R/W	description
P0:0xB7	TMS_CHOP_PD, TMS_CHOP_OP, TMS_VBG_TEST, TMS_VRBG	0x00	RW	Bit[7]: Not used Bit[6]: tms_chop_pd Bit[5]: tms_chop_op Bit[4]: tms_vbg_test Bit[3:0]: tms_vrbg

5.4 OSC [P0:0xF0 - P0:0xFC]

table 5-4 OSC registers (sheet 1 of 3)

address	register name	default value	R/W	description
P0:0xF0	CNT_TARGET_8LSB	0x80	RW	Bit[7:0]: cnt_target[7:0] Target mean low byte
P0:0xF1	CNT_MAX_8LSB	0x88	RW	Bit[7:0]: cnt_max[7:0] Target maximum low byte
P0:0xF2	CNT_MIN_8LSB	0x78	RW	Bit[7:0]: cnt_min[7:0] Target minimum low byte
P0:0xF3	CNT_TARGET_2MSB, CNT_MAX_2MSB, CNT_MIN_2MSB	0x15	RW	Bit[7:6]: Not used Bit[5:4]: cnt_target[9:8] Target mean high byte Bit[3:2]: cnt_max[9:8] Target maximum high byte Bit[1:0]: cnt_min[9:8] Target minimum high byte
P0:0xF4	OSC_CORNER	0x20	RW	Bit[7:6]: Not used Bit[5:0]: osc_corner Register configuration osc_corner

table 5-4 OSC registers (sheet 2 of 3)

address	register name	default value	R/W	description
P0:0xF5	TOP_CLK_SEL, OSC_OTP_EN, OSC_REG_EN, OSC_TEST_EN, OSC_CALI_EN	0x10	RW	Bit[7:6]: Not used Bit[5]: top_clk_sel osc_clk and ECLK select enable signal 0: Select osc_clk 1: Select ECLK Bit[4]: osc_otp_en Oscillator select OTP internal parameters 0: No selection 1: Select OTP internal parameters Bit[3]: Not used Bit[2]: osc_reg_en Oscillator select register configuration 0: No selection 1: Select P0:0xF4 parameter Bit[1]: osc_test_en Oscillator test mode 0: Turn off correction 1: Open test Bit[0]: osc_cali_en Oscillator correction mode 0: Turn off correction 1: Open correction
P0:0xF6	DELAY_CNT_8MSB	0xD0	RW	Bit[7:0]: delay_cnt[15:8] delay_cnt*8/144 µs Maximum value is 0xFFE0
P0:0xF7	DELAY_CNT_8LSB	0x07	RW	Bit[7:0]: delay_cnt[7:0]
P0:0xF8	OSC_DIVA, OSC_DIV, OSC_20M_EN, OSC_EN	–	RW	Bit[7:6]: osc_diva Bit[5:4]: osc_div Bit[3:2]: Not used Bit[1]: osc_20m_en Bit[0]: osc_en
P0:0xF9	OSC_CORNER	–	R	Bit[7:6]: Not used Bit[5:0]: osc_corner Store parameters corrected by oscillator This value needs to burn OTP
P0:0xFA	OSC_CNT_8LSB	–	R	Bit[7:0]: osc_cnt[7:0] Store count of successful correction of oscillator low byte
P0:0xFB	OSC_CNT_2MSB	–	R	Bit[7:2]: Not used Bit[1:0]: osc_cnt[9:8] Store count of successful correction of oscillator high byte

table 5-4 OSC registers (sheet 3 of 3)

address	register name	default value	R/W	description
P0:0xFC	CAL_DONE	–	R	Bit[7:3]: Not used Bit[2]: Oscillator correction fail indicator 1: Correction failed; output clock of oscillator fails to reach target value and osc_corner has been maximized Bit[1]: Oscillator correction fail indicator 1: Correction failed; osc_corner has reached minimum value, but output of oscillator does not reach target value Bit[0]: Oscillator correction success indicator 1: Correction is successful and output of oscillator reaches target value

5.5 CIS control [P1:0x01 - P1:0x4F, P1:0xCD - P1:0xF2]

table 5-5 CIS control registers (sheet 1 of 9)

address	register name	default value	R/W	description
P1:0x01	EXP_RPC_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: exp_rpc_en Enable of group hold 0: Disable 1: Enable
P1:0x02	RSVD	–	–	Reserved
P1:0x03	BUF_EXP_8MSB	0x01	RW	Bit[7:0]: buf_exp[15:8] Exposure time high byte in "H" unit 0x0001~0xFFFF: 1~65535
P1:0x04	BUF_EXP_8LSB	0x9A	RW	Bit[7:0]: buf_exp[7:0] Exposure time low byte in "H" unit 0x0001~0xFFFF: 1~65535
P1:0x05	VBLANK_BUF_8MSB	0x00	RW	Bit[7:0]: vblank_buf[15:8] Vertical blank high byte in "H" unit 0x0001~0xFFFF: 1~65535
P1:0x06	VBLANK_BUF_8LSB	0x00	RW	Bit[7:0]: vblank_buf[7:0] Vertical blank low byte in "H" unit 0x0001~0xFFFF: 1~65535

table 5-5 CIS control registers (sheet 2 of 9)

address	register name	default value	R/W	description
P1:0x07	RSVD	–	–	Reserved
P1:0x08	VPOS_BLANK	0x01	RW	Bit[7:4]: Not used Bit[3:0]: vpos_blank Time width between posedge of VSYNC and posedge of first HSYNC in "H" unit
P1:0x09	HBLANK_4MSB	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Hblank[11:8] Horizontal blank high byte in "timer_clk" unit 0x000~0xFFF: 0~4095
P1:0x0A	HBLANK_8LSB	0x00	RW	Bit[7:0]: Hblank[7:0] Horizontal blank low byte in "timer_clk" unit 0x000~0xFFF: 0~4095
P1:0x0B	EXTER_SYNC_CTL	0x00	RW	External Frame Synchronize Control Signal Bit[7]: exter_sync_inv Bit[6]: exter_frame_num_x256_en When enabled, 1 LSB of exter_sync_frame_num (P1:0x12) equals 256 frames 0: Disable 1: Enable Bit[5]: exter_del_en 0: Disable 1: Enable Bit[4]: exter_sync_manual_en Configure a positive value in this bit to trigger a sync output in master mode Bit[3]: exter_sync_auto_en Sensor in master mode will send sync signal every exter_sync_frame_num (P1:0x12) frames automatically 0: Disable 1: Enable Bit[2]: sync_no_wait_en Bit[1]: External sync slave mode 0: Disable 1: Enable Bit[0]: External sync master mode 0: Disable 1: Enable
P1:0x0C	EXTER_SYNC_OUT_WIDTH	0x00	RW	Bit[7:0]: Width of sync signal output when sensor is configured as master in "dac_clk" unit

table 5-5 CIS control registers (sheet 3 of 9)

address	register name	default value	R/W	description
P1:0x0D	SYNC_VB_EN, EXTER_SYNC_FRAME_ NUMBER_EN, FRAME_EXP_SEPARATE _EN, RPC_TEST, ROW_TEST, RPC_READ_END_EN, TEST_EN	0x02	RW	Bit[7]: Not used Bit[6]: sync_vb_en Bit[5]: exter_sync_frame_number_en Bit[4]: frame_exp_separate_en Bit[3]: rpc_test Bit[2]: row_test Bit[1]: rpc_read_end_en Bit[0]: test_en
P1:0x0E	FRAME_LENGTH_NUM_ 8MSB	0x04	RW	Bit[7:0]: Frame length for manual frame length setting[15:8] Used when register bit P1:0x0D[4] is enabled
P1:0x0F	FRAME_LENGTH_NUM_ 8LSB	0x50	RW	Bit[7:0]: Frame length for manual frame length setting[7:0] Used when register bit P1:0x0D[4] is enabled
P1:0x10	EXT_SYNC_TEST_RESULT, EXT_SYNC_TEST_DONE, EXT_SYNC_TEST_EN	0x00	RW	Bit[7:3]: Not used Bit[2]: ext_sync_test_result 0: External synchronization test is okay 1: External synchronization test is not okay Bit[1]: ext_sync_test_done 0: Test has not been done 1: Test has been done Bit[0]: ext_sync_test_en 0: Disable external synchronization test 1: Enable external synchronization test
P1:0x11	RSVD	–	–	Reserved
P1:0x12	EXTER_SYNC_FRAME_ NUM	0x0A	RW	Bit[7:0]: exter_sync_frame_num Interval frame number of auto external frame synchronize pulse

table 5-5 CIS control registers (sheet 4 of 9)

address	register name	default value	R/W	description
P1:0x13	SWITCH_DEL_FRAME_EN, PWD_DEL_FRAME_EN, UPDOWN_DEL_FRAME_EN, RST_DEL_EN, RST_COLROW_EN	0x00	RW	Bit[7:6]: Not used Bit[5]: switch_del_frame_en Control function for deleting bad frames when resolution switches 0: Disable 1: Enable Bit[4]: pwd_del_frame_en Control function for deleting bad frames during power down recovery 0: Disable 1: Enable Bit[3:2]: Not used Bit[1]: rst_del_en When enabled, sensor will delete first synchronized frame 0: Disable 1: Enable Bit[0]: rst_colrow_en Sensor column and row reset control 0: Disable 1: Enable
P1:0x14~ P1:0x22	RSVD	–	–	Reserved
P1:0x23	RPC1	–	R	Bit[7:0]: PGA gain control[7:0] Corresponding to register P1:0x24
P1:0x24	PGA_GAIN1_CTL	0x20	RW	Bit[7:0]: pga_gain1[7:0] Long frame RPC gain low byte pga_gain1 = {P1:0x3E[0], P1:0x24[7:0]} 0x000~0x1FF: 1x~31x
P1:0x25~ P1:0x30	RSVD	–	–	Reserved
P1:0x31	BUF_COMM_CTRL	0x00	RW	Bit[7]: Not used Bit[6]: hdr_mode Bit[5]: hdr_en Bit[4]: bypass_dsp Bit[3]: Not used Bit[2]: bin_en_m Bit[1]: bin_en_c Bit[0]: ana_window_en
P1:0x32~ P1:0x36	RSVD	–	–	Reserved

table 5-5 CIS control registers (sheet 5 of 9)

address	register name	default value	R/W	description
P1:0x37	DEL_FRAME_NUM2, DEL_FRAME_NUM	0x11	RW	Bit[7:6]: Not used Bit[5:4]: del_frame_num2 Control frame number to delete when resolution switching or power down recovery in short frame Bit[3:2]: Not used Bit[1:0]: del_frame_num Control frame number to delete when resolution switching or power down recovery long frame
P1:0x38	RSVD	–	–	Reserved
P1:0x39	ANA_V_DUMMY_SIZE	0x10	RW	Bit[7:0]: ana_v_dummy_size Specify vertical row number upward and downward of active readout area, respectively, for analog window mode
P1:0x3A	COL_ANA_ADDR_START_2MSB	0x00	RW	Bit[7:2]: Not used Bit[1:0]: col_ana_addr_start[9:8]
P1:0x3B	COL_ANA_ADDR_START_8LSB	0x00	RW	Bit[7:0]: col_ana_addr_start[7:0]
P1:0x3C	COL_ANA_ADDR_SIZE_2MSB	0x03	RW	Bit[7:2]: Not used Bit[1:0]: col_ana_addr_size[9:8]
P1:0x3D	COL_ANA_ADDR_SIZE_8LSB	0x3C	RW	Bit[7:0]: col_ana_addr_size[7:0]
P1:0x3E	SIG_GAIN1_EN, GAIN_2X_SEL, SCG_EN_SHORT, SCG_EN_LONG, PGA_GAIN2_MSB8, PGA_GAIN1_MSB8	0x10	RW	Bit[7:6]: Not used Bit[5]: sig_gain1_en Bit[4]: gain_2x_sel Bit[3]: scg_en_short Bit[2]: scg_en_long Bit[1]: pga_gain2[8] Short frame RPC gain high bit Bit[0]: pga_gain1[8] Long frame RPC gain high bit

table 5-5 CIS control registers (sheet 6 of 9)

address	register name	default value	R/W	description
P1:0x3F	BIN_EN_C_DIG, BIN_EN_M_DIG, COL_4X_BIN_EN, ROW_4X_BIN_EN_REG, BIN4_STEP_EN, FLIP/MIRROR	0x00	RW	Bit[7]: bin_en_c_dig Bit[6]: bin_en_m_dig Bit[5]: col_4x_bin_en Bit[4]: row_4x_bin_en_reg Bit[3]: bin4_step_en Bit[2]: Not used Bit[1:0]: Vertical flip/horizontal mirror 00: Normal (no flip) 01: Horizontal mirror 10: Vertical flip 11: Both horizontal mirror and vertical flip
P1:0x40	RSVD	–	–	Reserved
P1:0x41	VDELAY_BUF_8MSB	0x00	RW	Bit[7:0]: vdelay_buf[15:8] Vertical blank when exposure is greater than frame length high byte in "H" unit
P1:0x42	VDELAY_BUF_8LSB	0x00	RW	Bit[7:0]: vdelay_buf[7:0] Vertical blank when exposure is greater than frame length low byte in "H" unit
P1:0x43	EXTER_SYNC_DLY_NUM	0x00	RW	Bit[7:0]: exter_sync_dly_num
P1:0x44	RPC2	–	R	Bit[7:0]: PGA gain control short[7:0] Corresponding to register P1:0x45
P1:0x45	PGA_GAIN2_CTL	0x20	RW	Bit[7:0]: pga_gain2[7:0] Short frame RPC gain low byte pga_gain2 = {P1:0x3E[1], P1:0x45[7:0]} 0x000~0x1FF: 1x~31x
P1:0x46~ P1:0x47	RSVD	–	–	Reserved
P1:0x48	ROW_ANA_ADDR_START_ 3MSB	0x00	RW	Bit[7:3]: Not used Bit[2:0]: row_ana_addr_start[10:8]
P1:0x49	ROW_ANA_ADDR_START_ 8LSB	0x00	RW	Bit[7:0]: row_ana_addr_start[7:0]
P1:0x4A	ROW_ANA_ADDR_SIZE_ 3MSB	0x02	RW	Bit[7:3]: Not used Bit[2:0]: row_ana_addr_size[10:8]
P1:0x4B	ROW_ANA_ADDR_SIZE_ 8LSB	0xD8	RW	Bit[7:0]: row_ana_addr_size[7:0]

table 5-5 CIS control registers (sheet 7 of 9)

address	register name	default value	R/W	description
P1:0x4C	EXP2_8MSB	0x00	RW	Bit[7:0]: HDR short exposure time[15:8] in "H" unit 0x0001~0xFFFF: 1~65535
P1:0x4D	EXP2_8LSB	0x2E	RW	Bit[7:0]: HDR short exposure time[7:0] in "H" unit 0x0001~0xFFFF: 1~65535
P1:0x4E	FRAME_LENGTH_8MSB	–	R	Bit[7:0]: Frame length[15:8] in "H" unit
P1:0x4F	FRAME_LENGTH_8LSB	–	R	Bit[7:0]: Frame length[7:0] in "H" unit
P1:0xCD	DIG_GAIN_BUF_8LSB	0x40	RW	Bit[7:0]: dig_gain_buf[7:0] digital_gain for long frame dig_gain = {dig_gain_buf[10:8], dig_gain_buf[7:0]} 1x~32x, step: 1/64 0x40: 1x
P1:0xCE	DIG_GAIN2_BUF_8LSB	0x40	RW	Bit[7:0]: dig_gain2_buf[7:0] digital_gain for short frame dig_gain2 = {dig_gain2_buf[10:8], dig_gain2_buf[7:0]} 1x~32x, step: 1/64 0x40: 1x
P1:0xCF	DIG_GAIN_BUF_3MSB, DIG_GAIN2_BUF_3MSB	0x00	RW	Bit[7]: Not used Bit[6:4]: dig_gain_buf[10:8] Bit[3]: Not used Bit[2:0]: dig_gain2_buf[10:8]
P1:0xD0~ P1:0xD1	RSVD	–	–	Reserved
P1:0xD2	DARK_COL_ADDR_START_8LSB	0x10	RW	Bit[7:0]: dark_col_addr_start[7:0]
P1:0xD3~ P1:0xD7	RSVD	–	–	Reserved
P1:0xD8	SHORT_EXP_MAX_8MSB	0x01	RW	Bit[7:0]: short_exp_max[15:8] in HDR mode1
P1:0xD9	SHORT_EXP_MAX_8LSB	0x50	RW	Bit[7:0]: short_exp_max[7:0] in HDR mode1
P1:0xDA	HTS_8MSB	–	R	Bit[7:0]: HTS[15:8] Horizontal total size high byte
P1:0xDB	HTS_8LSB	–	R	Bit[7:0]: HTS[7:0] Horizontal total size low byte

table 5-5 CIS control registers (sheet 8 of 9)

address	register name	default value	R/W	description
P1:0xDC	ULP_PWD_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: ulp_pwd_en
P1:0xDD	ULP_START	0x00	RW	Bit[7:0]: ulp_start
P1:0xDE	ULP_END	0x00	RW	Bit[7:0]: ulp_end
P1:0xDF	RSVD	–	–	Reserved
P1:0xE0	EXP_BASE_CAL_8MSB	0x03	RW	Bit[7:0]: exp_base_cal[15:8]
P1:0xE1	EXP_BASE_CAL_8LSB	0x72	RW	Bit[7:0]: exp_base_cal[7:0]
P1:0xE2	EXP_STEP	0x00	RW	Bit[7:5]: Not used Bit[4:0]: exp_step
P1:0xE3	WAITING_ROW	0x00	RW	Bit[7:0]: waiting_row
P1:0xE4	QUICK_EXP_DEL	0x00	RW	Bit[7:1]: Not used Bit[0]: quick_exp_del
P1:0xE5	QUICK_EXP_ROWEND_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: quick_exp_rowend_en
P1:0xE6	RSVD	–	–	Reserved
P1:0xE7	REG_UPDATE_MODE, REG_UPDATE_CMD	0x00	RW	Bit[7:2]: Not used Bit[1]: reg_update_mode Bit[0]: reg_update_cmd
P1:0xE8	RSVD	–	–	Reserved
P1:0xE9	STROBE_CTRL	0x00	RW	Bit[7]: strobe_req Strobe start enable bit (long pulse or short pulse can trigger strobe) Bit[6]: strobe_inv Strobe output reverse enable (high efficiency) Bit[5:4]: xenon_width Xenon mode strobe pulse width 00: 1 line 01: 2 lines 10: 3 lines 11: 4 lines Bit[3]: strobe_level_ en Strobe output fixed level (controlled by 0x27 register) Bit[2]: led3_en Bit[1]: led12_en Bit[0]: xenon_en
P1:0xEA	STROBE_LEVEL	0x00	RW	Bit[7:1]: Not used Bit[0]: strobe_level

table 5-5 CIS control registers (sheet 9 of 9)

address	register name	default value	R/W	description
P1:0xEB	STROBE_DEL_NUM	0x00	RW	Bit[7:0]: strobe_del_num Delete frame register in LED12 mode can be configured directly to take effect
P1:0xEC	BUF_ADD_EXP_8MSB	0x02	RW	Bit[7:0]: buf_add_exp[15:8] Flash time high byte
P1:0xED	BUF_ADD_EXP_8LSB	0x20	RW	Bit[7:0]: buf_add_exp[7:0] Flash time low byte
P1:0xEF	CIS_BIST_ERROR_F, CIS_BIST_ERROR_S, CIS_BIST_DONE, MEM_STANDBY_CEN, CIS_BIST_EN	0x00	RW	Bit[7:6]: Not used Bit[5]: cis_bist_error_f (read only) Bit[4]: cis_bist_error_s (read only) Bit[3]: Not used Bit[2]: cis_bist_done Bit[1]: mem_standby_cen Bit[0]: cis_bist_en
P1:0xF0	RSVD	–	–	Reserved
P1:0xF1	PUMP_CLK_SEL	0x00	RW	Bit[7:1]: Not used Bit[0]: pump_clk_sel
P1:0xF2	REG_ECO	0x00	RW	Bit[7:0]: reg_eco

5.6 package [P2:0x53 - P1:0x54]

table 5-6 package registers

address	register name	default value	R/W	description
P2:0x53	OUTMODE1	0x00	RW	Bit[7:6]: Not used Bit[5]: unpro_raw_out_en Unprocessed RAW output enable 0: Disable unprocessed RAW 1: Enable unprocessed RAW Bit[4:0]: Not used
P2:0x54	OUTMODE2	0x00	RW	Bit[7:5]: Not used Bit[4]: domu_en Bit[3]: VSYNC inversion Bit[2]: HSYNC inversion Bit[1:0]: Not used

5.7 state [P2:0x55 - P2:0x5C]

table 5-7 state registers (sheet 1 of 2)

address	register name	default value	R/W	description
P2:0x55	FIX_STATE_EN2, FIX_STATE_EN, FIX_STATE_MODE2, FIX_STATE_MODE	0x00	RW	Bit[7:6]: Not used Bit[5]: fix_state_en2 Fix state enable in short frame 0: Disable fixed state 1: Enable fixed state Bit[4]: fix_state_en Fix state enable in long frame 0: Disable fixed state 1: Enable fixed state Bit[3]: Not used Bit[2]: fix_state_mode2 Fix which mode of state in short frame Bit[1]: Not used Bit[0]: fix_state_mode Fix which mode of state in long frame
P2:0x56	EXP_HEQ_DUMMY_8MSB	0x04	RW	Bit[7:0]: exp_heq_dummy[15:8] Exposure threshold between normal and lowlight in long frame high 8 bits
P2:0x57	EXP_HEQ_DUMMY_8LSB	0x60	RW	Bit[7:0]: exp_heq_dummy[7:0] Exposure threshold between normal and lowlight in long frame low 8 bits
P2:0x58	EXP2_HEQ_DUMMY_8MSB	0x04	RW	Bit[7:0]: exp2_heq_dummy[15:8] Exposure threshold between normal and lowlight in short frame high 8 bits
P2:0x59	EXP2_HEQ_DUMMY_8LSB	0x60	RW	Bit[7:0]: exp2_heq_dummy[7:0] Exposure threshold between normal and lowlight in short frame low 8 bits
P2:0x5A	RPC2_HEQ_DUMMY_8LSM	0x80	RW	Bit[7:0]: rpc2_heq_dummy[7:0] RPC threshold between normal and lowlight in short frame low 8 bits
P2:0x5B	RPC_HEQ_DUMMY_8LSM	0x80	RW	Bit[7:0]: rpc_heq_dummy[7:0] RPC threshold between normal and lowlight in long frame low 8 bits

table 5-7 state registers (sheet 2 of 2)

address	register name	default value	R/W	description
P2:0x5C	RPC2_HEQ_DUMMY_1MSB, RPC_HEQ_DUMMY_1MSB	0x00	RW	Bit[7:2]: Not used Bit[1]: rpc2_heq_dummy[8] RPC threshold between normal and lowlight in short frame high 1 bit Bit[0]: rpc_heq_dummy[8] RPC threshold between normal and lowlight in long frame high 1 bit

5.8 dynamic DPC [P2:0x00 - P2:0x5F]

table 5-8 dynamic DPC registers (sheet 1 of 4)

address	register name	default value	R/W	description
P2:0x00	ISP_CTRL_1_L	0x1B	RW	Bit[7]: Enable tail Bit[6]: Enable general tail Enable tailing cluster Bit[5]: Enable 3x3 cluster Bit[4]: Enable saturate cross cluster Bit[3]: Enable cross cluster Bit[2]: Manual mode enable Bit[1]: Black pixel enable Bit[0]: White pixel enable
P2:0x01	ISP_CTRL_1	0x94	RW	Bit[7:6]: Vertical number list[2] Bit[5:4]: Vertical number list[1] Bit[3:2]: Vertical number list[0] Bit[1]: Clip interpG Enable G clip Bit[0]: Enable share buffer No connect
P2:0x02	ISP_CTRL_2	0x2E	RW	Bit[7:6]: Not used Bit[5:4]: Bayer pattern order Bit[3:2]: EdgeOption Image boundary extend options Bit[1:0]: Vertical number list[3]
P2:0x03	ISP_CTRL_3	0x24	RW	Bit[7]: Not used Bit[6:3]: White pixel threshold list[0] Bit[2:0]: Maximum vertical number
P2:0x04	ISP_CTRL_4	0x12	RW	Bit[7:4]: White pixel threshold list[2] Bit[3:0]: White pixel threshold list[1]

table 5-8 dynamic DPC registers (sheet 2 of 4)

address	register name	default value	R/W	description
P2:0x05	ISP_CTRL_5	0x41	RW	Bit[7:4]: BThresRatio Dark pixel threshold ratio Bit[3:0]: White pixel threshold list[3]
P2:0x06	ISP_CTRL_6	0x48	RW	Bit[7:4]: Status threshold Bit[3:0]: MoreConnectionCaseThre Cluster threshold
P2:0x07	ISP_CTRL_7	0x84	RW	Bit[7:4]: MatchingThre Pattern match threshold Bit[3:0]: Status threshold step
P2:0x08	ISP_CTRL_8	0x40	RW	Bit[7:4]: Adaptive pattern step Bit[3:0]: Adaptive pattern threshold
P2:0x09	ISP_CTRL_9	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Saturate pixel threshold for clusters
P2:0x0A	ISP_CTRL_10	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Gain threshold list[0][4:0]
P2:0x0B	ISP_CTRL_11	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Gain threshold list[1][4:0]
P2:0x0C	ISP_CTRL_12	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Gain threshold list[2][4:0]
P2:0x0D	ISP_CTRL_13	0x0F	RW	Bit[7:0]: DPC level list[0]
P2:0x0E	ISP_CTRL_14	0xFD	RW	Bit[7:0]: DPC level list[1]
P2:0x0F	ISP_CTRL_15	0xF5	RW	Bit[7:0]: DPC level list[2]
P2:0x10	ISP_CTRL_16	0xF5	RW	Bit[7:0]: DPC level list[3]
P2:0x11~ P2:0x13	RSVD	–	–	Reserved
P2:0x14	ISP_CTRL_20	0x00	RW	Bit[7:5]: Recover clock gate disable Bit[4]: SRAM clock gate disable Bit[3]: Buffer control clock gate disable Bit[2]: Start frame clock gate disable Bit[1]: Clock gate disable Bit[0]: Pixel order manual enable
P2:0x15~ P2:0x17	RSVD	–	–	Reserved
P2:0x18	ISP_CTRL_24	–	R	Bit[7]: Not used Bit[6:0]: Bthre
P2:0x19	ISP_CTRL_25	–	R	Bit[7:5]: Not used Bit[4:0]: Wthre Wthre_list

table 5-8 dynamic DPC registers (sheet 3 of 4)

address	register name	default value	R/W	description
P2:0x1A	ISP_CTRL_26	–	R	Bit[7:5]: Not used Bit[4:0]: Thre1 matching_thre
P2:0x1B	ISP_CTRL_27	–	R	Bit[7:0]: Thre2 status_thre
P2:0x1C	ISP_CTRL_28	–	R	Bit[7]: Not used Bit[6:0]: Thre3adptive_pattern_thre
P2:0x1D	ISP_CTRL_29	–	R	Bit[7]: Not used Bit[6:0]: Thre4more_conn_case_thre
P2:0x1E	ISP_CTRL_30	–	R	Bit[7:4]: Level Bit[3:0]: Pconnected
P2:0x1F	ISP_CTRL_31	–	R	Bit[7:3]: Not used Bit[2:0]: Vnum
P2:0x20	ISP_CTRL_1_S	0x1B	RW	Bit[7]: Enable tail Bit[6]: Enable general tail Enable tailing cluster Bit[5]: Enable 3x3 cluster Bit[4]: Enable saturate cross cluster Bit[3]: Enable cross cluster Bit[2]: Manual mode enable Bit[1]: Black pixel enable Bit[0]: White pixel enable
P2:0x21~ P2:0x3F	RSVD	–	–	Reserved
P2:0x40	CFA_PTN, CEN_GLOBAL, SCLK_GT_DIS	0x12	RW	Bit[7:6]: Not used Bit[5:4]: cfa_ptn Bit[3:2]: Not used Bit[1]: cen_global Bit[0]: sclk_gt_dis
P2:0x41~ P2:0x42	RSVD	–	–	Reserved
P2:0x43	HSIZE_DPC_3MSB	0x07	RW	Bit[7:3]: Not used Bit[2:0]: hsize_dpc[10:8]
P2:0x44	HSIZE_DPC_8LSB	0x88	RW	Bit[7:0]: hsize_dpc[7:0]
P2:0x45	GAINLIST_0_L_4LSB, GAINLIST_1_L_4LSB	0x3F	RW	Bit[7:4]: Gain threshold list_l[0][3:0] Bit[3:0]: Gain threshold list_l[1][3:0]
P2:0x46	GAINLIST_2_L_4LSB, GAINLIST_2_S_4LSB	0xFF	RW	Bit[7:4]: Gain threshold list_l[2][3:0] Bit[3:0]: Gain threshold list_s[2][3:0]
P2:0x47	GAINLIST_0_S_4LSB, GAINLIST_1_S_4LSB	0x3F	RW	Bit[7:4]: Gain threshold list_s[0][3:0] Bit[3:0]: Gain threshold list_s[1][3:0]
P2:0x48~ P2:0x51	RSVD	–	–	Reserved

table 5-8 dynamic DPC registers (sheet 4 of 4)

address	register name	default value	R/W	description
P2:0x52	ISP_MODE	0xFE	RW	Bit[7]: dpc_s_en Dynamic DPC enable in short frame 0: Disable 1: Enable Bit[6:5]: Not used Bit[4]: dpc_l_en Dynamic DPC enable in long frame 0: Disable 1: Enable Bit[3]: demo_en demo_gf power down enable 0: Enable demo_gf power down 1: Disable demo_gf power down Bit[2:1]: Not used Bit[0]: dp_pos_en 0: Disable 1: Enable read OTP DPC data
P2:0x53~ P2:0x5C	RSVD	–	–	Reserved
P2:0x5D	BAYER_ORDER	0x01	RW	Bit[7:2]: Not used Bit[1:0]: bayer_order Bayer RAW order 00: GBGB 01: BGBG 10: GRGR 11: RGRG
P2:0x5E	AUTO_BR_FIRST, BR_FIRST	0x02	RW	Bit[7:2]: Not used Bit[1]: auto_first_en Auto br_first enable whether flip or mirror 0: Disable auto_br_first 1: Enable auto_br_first Bit[0]: br_first odd_flag set 0: odd_flag normal 1: odd_flag reverse
P2:0x5F	BIST	0x00	RW	Bit[7:1]: Not used Bit[0]: BIST

5.9 OTP BPC [P2:0x60 - P2:0x63, P4:0x12 - P4:0x15, P4:0x33 - P4:0x36]

table 5-9 OTP BPC registers

address	register name	default value	R/W	description
P2:0x60	LSC_BPC_EN	0x0F	RW	Bit[7:4]: Not used Bit[3]: OTP bpc_short enable in outdoor Bit[2]: OTP bpc_short enable in lowlight Bit[1]: OTP BPC enable in outdoor Bit[0]: OTP BPC enable in lowlight
P2:0x61	RSVD	–	–	Reserved
P2:0x62	ROW_START_8LSB	0x01	RW	Bit[7:0]: row_start[7:0] BPC start row number low 8 bits
P2:0x63	ROW_START_3MSB	0x00	RW	Bit[7:3]: Not used Bit[2:0]: row_start[10:8] BPC start row number high 3 bits
P4:0x12	ISP_REGF_12	0x10	RW	Bit[7:0]: bpc_dif_thr_outdoor BPC grad difference threshold in outdoor in long frame
P4:0x13	ISP_REGF_13	0x10	RW	Bit[7:0]: bpc_dif_thr_low BPC grad difference threshold in lowlight in long frame
P4:0x14	ISP_REGF_14	0x10	RW	Bit[7:0]: bpc_grad_thr_outdoor BPC edge grad threshold in outdoor in long frame
P4:0x15	ISP_REGF_15	0x10	RW	Bit[7:0]: bpc_grad_thr_low BPC edge grad threshold in lowlight in long frame
P4:0x33	ISP_REGF_33	0x10	RW	Bit[7:0]: bpc_dif_thr_outdoor BPC grad difference threshold in outdoor in short frame
P4:0x34	ISP_REGF_34	0x10	RW	Bit[7:0]: bpc_dif_thr_low BPC grad difference threshold in lowlight in short frame
P4:0x35	ISP_REGF_35	0x10	RW	Bit[7:0]: bpc_grad_thr_outdoor BPC edge grad threshold in outdoor in short frame
P4:0x36	ISP_REGF_36	0x10	RW	Bit[7:0]: bpc_grad_thr_low BPC edge grad threshold in lowlight in short frame

5.10 demo_sif [P2:0xA0 - P2:0xFA, P4:0x16 - P4:0x32]

table 5-10 demo_sif registers (sheet 1 of 4)

address	register name	default value	R/W	description
P2:0xA0	DEM_V_START_3MSB	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Image vertical start[10:8]
P2:0xA1	DEM_V_START_8LSB	0x00	RW	Bit[7:0]: Image vertical start[7:0]
P2:0xA2	DEM_V_SIZE_3MSB	0x04	RW	Bit[7:3]: Not used Bit[2:0]: Image vertical size[10:8]
P2:0xA3	DEM_V_SIZE_8LSB	0x48	RW	Bit[7:0]: Image vertical size[7:0]
P2:0xA4	DEM_H_START_3MSB	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Image horizontal start[10:8]
P2:0xA5	DEM_H_START_8LSB	0x00	RW	Bit[7:0]: Image horizontal start[7:0]
P2:0xA6	DEM_H_SIZE_3MSB	0x07	RW	Bit[7:3]: Not used Bit[2:0]: Image horizontal size[10:8]
P2:0xA7	DEM_H_SIZE_8LSB	0x90	RW	Bit[7:0]: Image horizontal size[7:0]
P2:0xA8	TEMP_TONE_EN, TEMP_SIF_EN	0x00	RW	Bit[7:2]: Not used Bit[1]: temp_tone_en Bit[0]: temp_sif_en
P2:0xA9	TEMP_SIF_R_START_ 3MSB	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Image vertical start[10:8]
P2:0xAA	TEMP_SIF_R_START_8LSB	0x00	RW	Bit[7:0]: Image vertical start[7:0]
P2:0xAB	TEMP_SIF_C_START_ 3MSB	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Image horizontal start[10:8]
P2:0xAC	TEMP_SIF_C_START_8LSB	0x00	RW	Bit[7:0]: Image horizontal start[7:0]
P2:0xAD	TEMP_SIF_R_SIZE_3MSB	0x04	RW	Bit[7:3]: Not used Bit[2:0]: Image vertical size[10:8]
P2:0xAE	TEMP_SIF_R_SIZE_8LSB	0x48	RW	Bit[7:0]: Image vertical size[7:0]
P2:0xAF	TEMP_SIF_C_SIZE_3MSB	0x07	RW	Bit[7:3]: Not used Bit[2:0]: Image half horizontal size[10:8]
P2:0xB0	TEMP_SIF_C_SIZE_8LSB	0x90	RW	Bit[7:0]: Image half horizontal size[7:0]
P2:0xB1	TEMP_TONE	0x00	RW	Bit[7:0]: temp_tone
P2:0xB2~ P2:0xF8	RSVD	–	–	Reserved

table 5-10 demo_sif registers (sheet 2 of 4)

address	register name	default value	R/W	description
P2:0xF9	DC_TEST_EN, DC_MIST_SET, DC_DATA_SET_2LSB	0x00	RW	Bit[7:6]: Not used Bit[5]: Enable test pad Bit[4]: Test VSYNC pad Bit[3]: Test HSYNC pad Bit[2]: Not used Bit[1:0]: For test data pad[1:0]
P2:0xFA	DC_DATA_SET_8MSB	0x00	RW	Bit[7:0]: For test data pad[15:2]
P4:0x16	POSITION_MSB	0x00	RW	Bit[7]: For test OTP DPC point 3 type, xyt_32 position[2] Bit[6]: For test OTP DPC point 3 type, xyt_31 position[2] Bit[5]: For test OTP DPC point 3 type, xyt_23 position[2] Bit[4]: For test OTP DPC point 3 type, xyt_22 position[2] Bit[3]: For test OTP DPC point 3 type, xyt_21 position[2] Bit[2]: For test OTP DPC point 3 type, xyt_13 position[2] Bit[1]: For test OTP DPC point 3 type, xyt_12 position[2] Bit[0]: For test OTP DPC point 3 type, xyt_11 position[2]
P4:0x17	DP_REGF_EN, POSITION_MSB	0x00	RW	Bit[7:5]: Not used Bit[4]: For test OTP DPC point 3 type, xyt_33 position[2] Bit[3:1]: Not used Bit[0]: Enable test OTP DPC
P4:0x18	DP_XYT_11_REG1	0x00	RW	Bit[7:0]: For test OTP DPC point 1 coordinates of x[7:0]
P4:0x19	DP_XYT_11_REG2	0x00	RW	Bit[7:0]: For test OTP DPC point 1 coordinates of y[7:0]
P4:0x1A	DP_XYT_11_REG3	0x00	RW	Bit[7:6]: For test OTP DPC point 1 type Bit[5:3]: For test OTP DPC point 1 coordinates of x 2[10:8] Bit[2:0]: For test OTP DPC point 1 coordinates of y[10:8]
P4:0x1B	DP_XYT_12_REG1	0x00	RW	Bit[7:0]: For test OTP DPC point 2 coordinates of x[7:0]
P4:0x1C	DP_XYT_12_REG2	0x00	RW	Bit[7:0]: For test OTP DPC point 2 coordinates of y[7:0]

table 5-10 demo_sif registers (sheet 3 of 4)

address	register name	default value	R/W	description
P4:0x1D	DP_XYT_12_REG3	0x00	RW	Bit[7:6]: For test OTP DPC point 2 type Bit[5:3]: For test OTP DPC point 2 coordinates of x[10:8] Bit[2:0]: For test OTP DPC point 2 coordinates of y[10:8]
P4:0x1E	DP_XYT_13_REG1	0x00	RW	Bit[7:0]: For test OTP DPC point 3 coordinates of x[7:0]
P4:0x1F	DP_XYT_13_REG2	0x00	RW	Bit[7:0]: For test OTP DPC point 3 coordinates of y[7:0]
P4:0x20	DP_XYT_13_REG3	0x00	RW	Bit[7:6]: For test OTP DPC point 3 type Bit[5:3]: For test OTP DPC point 3 coordinates of x[10:8] Bit[2:0]: For test OTP DPC point 3 coordinates of y[10:8]
P4:0x21	DP_XYT_21_REG1	0x00	RW	Bit[7:0]: For test OTP DPC point 1 coordinates of x[7:0]
P4:0x22	DP_XYT_21_REG2	0x00	RW	Bit[7:0]: For test OTP DPC point 1 coordinates of y[7:0]
P4:0x23	DP_XYT_21_REG3	0x00	RW	Bit[7:6]: For test OTP DPC point 1 type Bit[5:3]: For test OTP DPC point 1 coordinates of x[10:8] Bit[2:0]: For test OTP DPC point 1 coordinates of y[10:8]
P4:0x24	DP_XYT_22_REG1	0x00	RW	Bit[7:0]: For test OTP DPC point 2 coordinates of x[7:0]
P4:0x25	DP_XYT_22_REG2	0x00	RW	Bit[7:0]: For test OTP DPC point 2 coordinates of y[7:0]
P4:0x26	DP_XYT_22_REG3	0x00	RW	Bit[7:6]: For test OTP DPC point 2 type Bit[5:3]: For test OTP DPC point 2 coordinates of x[10:8] Bit[2:0]: For test OTP DPC point 2 coordinates of y[10:8]
P4:0x27	DP_XYT_23_REG1	0x00	RW	Bit[7:0]: For test OTP DPC point 3 coordinates of x[7:0]
P4:0x28	DP_XYT_23_REG2	0x00	RW	Bit[7:0]: For test OTP DPC point 3 coordinates of y[7:0]
P4:0x29	DP_XYT_23_REG3	0x00	RW	Bit[7:6]: For test OTP DPC point 3 type Bit[5:3]: For test OTP DPC point 3 coordinates of x[10:8] Bit[2:0]: For test OTP DPC point 3 coordinates of y[10:8]

table 5-10 demo_sif registers (sheet 4 of 4)

address	register name	default value	R/W	description
P4:0x2A	DP_XYT_31_REG1	0x00	RW	Bit[7:0]: For test OTP DPC point 1 coordinates of x[7:0]
P4:0x2B	DP_XYT_31_REG2	0x00	RW	Bit[7:0]: For test OTP DPC point 1 coordinates of y[7:0]
P4:0x2C	DP_XYT_31_REG3	0x00	RW	Bit[7:6]: For test OTP DPC point 1 type Bit[5:3]: For test OTP DPC point 1 coordinates of x[10:8] Bit[2:0]: For test OTP DPC point 1 coordinates of y[10:8]
P4:0x2D	DP_XYT_32_REG1	0x00	RW	Bit[7:0]: For test OTP DPC point 2 coordinates of x[7:0]
P4:0x2E	DP_XYT_32_REG2	0x00	RW	Bit[7:0]: For test OTP DPC point 2 coordinates of y[7:0]
P4:0x2F	DP_XYT_32_REG3	0x00	RW	Bit[7:6]: For test OTP DPC point 2 type Bit[5:3]: For test OTP DPC point 2 coordinates of x[10:8] Bit[2:0]: For test OTP DPC point 2 coordinates of y[10:8]
P4:0x30	DP_XYT_33_REG1	0x00	RW	Bit[7:0]: For test OTP DPC point 3 coordinates of x[7:0]
P4:0x31	DP_XYT_33_REG2	0x00	RW	Bit[7:0]: For test OTP DPC point 3 coordinates of y[7:0]
P4:0x32	DP_XYT_33_REG3	0x00	RW	Bit[7:6]: For test OTP DPC point 3 type Bit[5:3]: For test OTP DPC point 3 coordinates of x[10:8] Bit[2:0]: For test OTP DPC point 3 coordinates of y[10:8]

5.11 BLC [P2:0x64 - P2:0x9F]

table 5-11 BLC registers (sheet 1 of 5)

address	register name	default value	R/W	description
P2:0x64	TPM_DATA_MAX_8MSB	0x10	RW	Bit[7:0]: tpm_data_max[15:8]
P2:0x65	TPM_DATA_MAX_8LSB	0x00	RW	Bit[7:0]: tpm_data_max[7:0]
P2:0x66	DC_LEVEL_LIMIT_DATA_8LSB	0x20	RW	Bit[7:0]: Limitation of DC[7:0]
P2:0x67	DC_LEVEL_LIMIT_DATA_2MSB	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Limitation of DC[9:8]

table 5-11 BLC registers (sheet 2 of 5)

address	register name	default value	R/W	description
P2:0x68	RANDOM_SEL, ADC_HIGH_8BIT, DC_LEVEL_LIMIT_EN	0x02	RW	Bit[7:3]: Not used Bit[2]: random_sel Bit[1]: adc_high_8bit Bit[0]: dc_level_limit_en
P2:0x69	BLC_LIMIT_DATA_8LSB	0xE8	RW	Bit[7:0]: Limitation of data output[7:0]
P2:0x6A	BLC_LIMIT_DATA_2MSB	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Limitation of data output[9:8]
P2:0x6B	KSCG_EN, CIS_DATA_CLAMP_EN, CIS_DATA_RAND_EN	0x00	RW	Bit[7:3]: Not used Bit[2]: kscg_en Bit[1]: cis_data_clamp_en Bit[0]: cis_data_rand_en
P2:0x6B	RSVD	–	–	Reserved
P2:0x6D	ABL	0x00	RW	Bit[7]: blc_test_en 0: Low 10-bit output mode 1: High 10-bit output mode Bit[6]: blc_filter_en 0: Dark row median filter disable 1: Dark row median filter enable Bit[5]: ob2_en 0: OB2 disable 1: OB2 enable Bit[4]: blc_bpc_en 0: Dark row BPC disable 1: Dark row BPC enable Bit[3]: random_en 0: Add random value disable 1: Add random value enable Bit[2:1]: blc_mode 00: 1 frame average mode 01: 4 frames average mode 10: 8 frames average mode 11: 1 frame average mode Bit[0]: blc_en 0: Black level disable 1: Black level enable
P2:0x6E	ABL_TRIGGER	0x00	RW	Bit[7]: scg_en_trigger Bit[6]: tpm_trigger Bit[5]: Auto BLC enable Bit[4]: Gain trigger Bit[3]: Exposure trigger Bit[2]: mean_trigger Bit[1]: Refresh BLC sum Bit[0]: Manual trigger

table 5-11 BLC registers (sheet 3 of 5)

address	register name	default value	R/W	description
P2:0x6F	TRIG_FRAMECOUNT	0x02	RW	Bit[7:4]: Not used Bit[3]: trig_framecount Bit[2:0]: Not used
P2:0x70	BLC_DATA_SEL, BL_POSITION_SET2, BL_POSITION_SET	0x00	RW	Bit[7:5]: Not used Bit[4]: blc_data_sel Bit[3:2]: bl_position_set2 Bit[1:0]: bl_position_set
P2:0x71	BL_POSITION1_SET2, BL_POSITION1_SET	0x00	RW	Bit[7:4]: Not used Bit[3:2]: bl_position1_set2 Bit[1:0]: bl_position1_set
P2:0x72	BLUE_SUBOFFSET_8LSB	0x00	RW	Bit[7:0]: Black level offset, blue channel[7:0] Total register is 9 bits with MSB at P2:0x76[7]
P2:0x73	RED_SUBOFFSET_8LSB	0x00	RW	Bit[7:0]: Black level offset, red channel[7:0] Total register is 9 bits with MSB at P2:0x76[6]
P2:0x74	GR_SUBOFFSET_8LSB	0x00	RW	Bit[7:0]: Black level offset, Gr channel[7:0] Total register is 9 bits with MSB at P2:0x76[5]
P2:0x75	GB_SUBOFFSET_8LSB	0x00	RW	Bit[7:0]: Black level offset, Gb channel[7:0] Total register is 9 bits with MSB at P2:0x76[4]
P2:0x76	BLUE_SUBOFFSET_1MSB, RED_SUBOFFSET_1MSB, GR_SUBOFFSET_1MSB, GB_SUBOFFSET_1MSB	0x00	RW	Bit[7]: Black level offset, blue channel[8] High 1-bit, which is sign bit, and low bits are at P2:0x72[7:0] Bit[6]: Black level offset, red channel[8] High 1-bit, which is sign bit, and low bits are at P2:0x73[7:0] Bit[5]: Black level offset, Gr channel[8] High 1-bit, which is sign bit, and low bits are at P2:0x74[7:0] Bit[4]: Black level offset, Gb channel[8] High 1-bit, which is sign bit, and low bits are at P2:0x75[7:0] Bit[3:0]: Not used
P2:0x77	BLC_CHANNEL_SEL	0x07	RW	Bit[7:3]: Not used Bit[2:0]: blc_channel_sel

table 5-11 BLC registers (sheet 4 of 5)

address	register name	default value	R/W	description
P2:0x78	BLC_EXP_BLUE	0x80	RW	Bit[7:0]: blc_exp_blue[7:0]
P2:0x79	BLC_EXP_RED	0x80	RW	Bit[7:0]: blc_exp_red[7:0]
P2:0x7A	BLC_EXP_GR	0x80	RW	Bit[7:0]: blc_exp_gr[7:0]
P2:0x7B	BLC_EXP_GB	0x80	RW	Bit[7:0]: blc_exp_gb[7:0]
P2:0x7C	BLC_RPC_BLUE	0x00	RW	Bit[7:6]: Not used Bit[5:0]: blc_rpc_blue
P2:0x7D	BLC_RPC_RED	0x00	RW	Bit[7:6]: Not used Bit[5:0]: blc_rpc_red
P2:0x7E	BLC_RPC_GR	0x00	RW	Bit[7:6]: Not used Bit[5:0]: blc_rpc_gr
P2:0x7F	BLC_RPC_GB	0x00	RW	Bit[7:6]: Not used Bit[5:0]: blc_rpc_gb
P2:0x80	BLC_BPC_TH_P_8LSB	0x40	RW	Bit[7:0]: blc_bpc_th_p[7:0] Black level positive threshold for bad pixels, encoded in absolute value
P2:0x81	BLC_BPC_TH_N_8LSB	0xC0	RW	Bit[7:0]: blc_bpc_th_n[7:0] Black level negative threshold for bad pixels, encoded in absolute value
P2:0x82	BLC_MEAN_MAX	0x00	RW	Bit[7:0]: Black level shift, blue channel 0x00~0xFF: 0~255
P2:0x83	BLC_BPC_IN_P_8LSB	0xC0	RW	Bit[7:0]: blc_bpc_in_p[7:0] Black level positive threshold for bad pixels, encoded in absolute value
P2:0x84	BLC_BPC_IN_N_8LSB	0xC0	RW	Bit[7:0]: blc_bpc_in_n[7:0] Black level negative threshold for bad pixels, encoded in absolute value
P2:0x85	GAIN_LIMIT	0x0C	RW	Bit[7:6]: Not used Bit[5:0]: Black level shift Gb channel 0x00~0xFF: 0~255
P2:0x86	BLACK_LEVEL_GB_8LSB	–	R	Bit[7:0]: black_level_gb[7:0]
P2:0x87	BLACK_LEVEL_B_8LSB	–	R	Bit[7:0]: black_level_b[7:0]
P2:0x88	BLACK_LEVEL_R_8LSB	–	R	Bit[7:0]: black_level_r[7:0]
P2:0x89	BLACK_LEVEL_GR_8LSB	–	R	Bit[7:0]: black_level_gr[7:0]
P2:0x8A	BLACK_LEVEL_GB_8MSB	–	R	Bit[7:0]: black_level_gb[15:8]

table 5-11 BLC registers (sheet 5 of 5)

address	register name	default value	R/W	description
P2:0x8B	BLACK_LEVEL_B_8MSB	–	R	Bit[7:0]: black_level_b[15:8]
P2:0x8C	BLACK_LEVEL_R_8MSB	–	R	Bit[7:0]: black_level_r[15:8]
P2:0x8D	BLACK_LEVEL_GR_8MSB	–	R	Bit[7:0]: black_level_gr[15:8]
P2:0x8E	BLACK1_LEVEL_GB_8LSB	–	R	Bit[7:0]: black1_level_gb[7:0]
P2:0x8F	BLACK1_LEVEL_B_8LSB	–	R	Bit[7:0]: black1_level_b[7:0]
P2:0x90	BLACK1_LEVEL_R_8LSB	–	R	Bit[7:0]: black1_level_r[7:0]
P2:0x91	BLACK1_LEVEL_GR_8LSB	–	R	Bit[7:0]: black1_level_gr[7:0]
P2:0x92	BLACK1_LEVEL_GB_8MSB	–	R	Bit[7:0]: black1_level_gb[15:8]
P2:0x93	BLACK1_LEVEL_B_8MSB	–	R	Bit[7:0]: black1_level_b[15:8]
P2:0x94	BLACK1_LEVEL_R_8MSB	–	R	Bit[7:0]: black1_level_r[15:8]
P2:0x95	BLACK1_LEVEL_GR_8MSB	–	R	Bit[7:0]: black1_level_gr[15:8]
P0:0x96	RSVD	–	–	Reserved
P2:0x97	BLC_EXP_BLUE1	0x80	RW	Bit[7:0]: blc_exp_blue1[7:0]
P2:0x98	BLC_EXP_RED1	0x80	RW	Bit[7:0]: blc_exp_red1[7:0]
P2:0x99	BLC_EXP_GR1	0x80	RW	Bit[7:0]: blc_exp_gr1[7:0]
P2:0x9A	BLC_EXP_GB1	0x80	RW	Bit[7:0]: blc_exp_gb1[7:0]
P2:0x9B	BLC_RPC_BLUE1	0x00	RW	Bit[7:6]: Not used Bit[5:0]: blc_rpc_blue1
P2:0x9C	BLC_RPC_RED1	0x00	RW	Bit[7:6]: Not used Bit[5:0]: blc_rpc_red1
P2:0x9D	BLC_RPC_GR1	0x00	RW	Bit[7:6]: Not used Bit[5:0]: blc_rpc_gr1
P2:0x9E	BLC_RPC_GB1	0x00	RW	Bit[7:6]: Not used Bit[5:0]: blc_rpc_gb1
P2:0x9F	BLC_MEAN_MAX1	0x00	RW	Bit[7:0]: blc_mean_max1

5.12 OTP IP [P3:0xE0 - P3:0xE6]

table 5-12 OTP IP registers

address	register name	default value	R/W	description
P3:0xE0	TPGM_8LSB	0xEA	RW	Bit[7:0]: OTP programming time set[7:0]
P3:0xE1	TPGM_6MSB	0x01	RW	Bit[7:6]: Not used Bit[5:0]: OTP programming time set[13:8]
P3:0xE2	TSUP_CS	0x01	RW	Bit[7:0]: OTP operation address setup time set
P3:0xE3	THP_CS	0x01	RW	Bit[7:0]: OTP operation address hold time set
P3:0xE4	TSQ	0x02	RW	Bit[7:0]: OTP access time set
P3:0xE5	TRD	0x17	RW	Bit[7:0]: OTP read time set
P3:0xE6	TGAP	0x04	RW	Bit[7:0]: Time gap set Between steady output data to read enable signals, this will improve timing

5.13 OTP status [P3:0xE7, P3:0xEC]

table 5-13 OTP status registers

address	register name	default value	R/W	description
P3:0xE7	PGM_PERMIT	0x00	RW	Bit[7:1]: Not used Bit[0]: OTP programming permits flag 0: Forbid PGM process 1: Permits PGM process
P3:0xEC	OTP_PGM_FLAG, READ_FLAG, BAT_RD_FLAG, OTP_BUSY	–	R	Bit[7:4]: Not used Bit[3]: otp_pgm_flag Bit[2]: read_flag Bit[1]: bat_rd_flag Bit[0]: otp_busy Note: All flags are read only

5.14 OTP mode [P3:0xD0, P3:0xE8, P3:0xEA - P3:0xEB]

table 5-14 OTP mode registers

address	register name	default value	R/W	description
P3:0xD0	PAGE_HALF_FLAG, OTP_BATCH_EN	0x00	RW	Bit[7:5]: Not used Bit[4]: page_half_flag Select signal of OTP batch program address 0: Select OTP 0x00~0x3F to program 1: Select OTP 0x40~0x7F to program Bit[3:1]: Not used Bit[0]: otp_batch_en 0: Disable batch program 1: Start batch program
P3:0xE8	PGM_PAGE, OTP_PGM_EN	0x00	RW	Bit[7]: Not used Bit[6:4]: PGM page select Bit[3:1]: Not used Bit[0]: Start programming OTP Warning: Before using this command, make sure that OTP is not busy and exact address has been written to a suitable value when program operation is permitted
P3:0xEA	DATA_BYT_WR	0x00	RW	Bit[7:0]: data_byt_wr Data required to program to OTP in byte program mode
P3:0xEB	ADDR_BYT_WR	0x00	RW	Bit[7:0]: addr_byt_wr OTP cell address in byte program mode

5.15 TPM [P6:0x00 - P6:0x23]

table 5-15 TPM registers (sheet 1 of 3)

address	register name	default value	R/W	description
P6:0x00	R_TMP_SLOPE_H	0x05	RW	Bit[7:0]: TM slope[15:8]
P6:0x01	R_TMP_SLOPE_L	0x19	RW	Bit[7:0]: TM slope[7:0]
P6:0x02	R_TMP_OFFSET_3	0xFD	RW	Bit[7:0]: TM offset[31:24]
P6:0x03	R_TMP_OFFSET_2	0xD1	RW	Bit[7:0]: TM offset[23:16]
P6:0x04	R_TMP_OFFSET_1	0xFF	RW	Bit[7:0]: TM offset[15:8]
P6:0x05	R_TMP_OFFSET_0	0xFF	RW	Bit[7:0]: TM offset[7:0]
P6:0x06	R_DIV	0x08	RW	Bit[7:0]: p_clk_l clock divide option Output sampling clock
P6:0x07	R_CNT_BIT	0x07	RW	Bit[7:3]: Not used Bit[2:0]: tm_number of out sampling cycles Db period 000: 2^9 sampling cycles 001: 2^{10} sampling cycles 010: 2^{11} sampling cycles 011: 2^{12} sampling cycles 100: 2^{13} sampling cycles 101: 2^{14} sampling cycles 110: 2^{15} sampling cycles 111: 2^{16} sampling cycles
P6:0x08~ P6:0x09	RSVD	–	–	Reserved
P6:0x0A	R_OTP_CTRL_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: OTP control to load slope and offset enable
P6:0x0B	R_SOF_UPDATE_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: Start of frame (SOF) update enable 0: sof_i is invalid 1: sof_i is in effect
P6:0x0C	R_SHIFT_BIT	0x05	RW	Bit[7:5]: Not used Bit[4:0]: Shift bit value
P6:0x0D	R_PD_TPM_SNR	0x00	RW	Bit[7:1]: Not used Bit[0]: TM power down

table 5-15 TPM registers (sheet 2 of 3)

address	register name	default value	R/W	description
P6:0x0E	R_DIV_SEL	0x00	RW	Bit[7:1]: Not used Bit[0]: Div select When r_mul_div_sel (P6:0x0F) = 1 0: Result is db_real/slope 1: Result is slope/db_real
P6:0x0F	R_MUL_DIV_SEL	0x00	RW	Bit[7:1]: Not used Bit[0]: r_mul_div_sel Mul and div select 0: Do 16-bit multiplication, result is 32 bits 1: Do 16-bit division, result is 0 for high 16 bits and quotient for low 16 bits
P6:0x10	R_TPM_MIN	0x00	RW	Bit[7:0]: tpm_min Minimum value for TM
P6:0x11	R_TPM_MAX	0xFF	RW	Bit[7:0]: tpm_max Maximum value for TM
P6:0x12	R_TPM_F_EN	0x00	RW	Bit[7:0]: tpm_f_en (self clearing) When = 1, latch_en is basically always working
P6:0x13	R_TPM_INT_RDOUT	–	R	Bit[7:0]: tpm_int_rout Read out TPM integer rdout
P6:0x14	R_TPM_DEC_RDOUT	–	R	Bit[7:0]: tpm_dec_rout Read out TPM decimal rdout
P6:0x15	R_TPM_INT	–	R	Bit[7:0]: tpm_int Read out TPM integer
P6:0x16	R_TPM_DEC	–	R	Bit[7:0]: tpm_dec Read out TPM decimal
P6:0x17	R_DB_NUM	–	R	Bit[7:0]: Read out db number
P6:0x18	R_DB_REAL_H	–	R	Bit[7:0]: Read out db real[15:8]
P6:0x19	R_DB_REAL_L	–	R	Bit[7:0]: Read out db real[7:0]
P6:0x1A	R_TPM_ABS_3	–	R	Bit[7:0]: tpm_abs[31:24] Read out TPM abs
P6:0x1B	R_TPM_ABS_2	–	R	Bit[7:0]: tpm_abs[23:16] Read out TPM abs
P6:0x1C	R_TPM_ABS_1	–	R	Bit[7:0]: tpm_abs[15:8] Read out TPM abs
P6:0x1D	R_TPM_ABS_0	–	R	Bit[7:0]: tpm_abs[7:0] Read out TPM abs

table 5-15 TPM registers (sheet 3 of 3)

address	register name	default value	R/W	description
P6:0x1E	R_TPM_ADD_ABS_3	–	R	Bit[7:0]: tpm_add_abs[31:24] Read out TPM add abs
P6:0x1F	R_TPM_ADD_ABS_2	–	R	Bit[7:0]: tpm_add_abs[23:16] Read out TPM add abs
P6:0x20	R_TPM_ADD_ABS_1	–	R	Bit[7:0]: tpm_add_abs[15:8] Read out TPM add abs
P6:0x21	R_TPM_ADD_ABS_0	–	R	Bit[7:0]: tpm_add_abs[7:0] Read out TPM add abs
P6:0x22	R_TPM_ADD_H	–	R	Bit[7:0]: tpm_value[15:8] Read out TPM value
P6:0x23	R_TPM_ADD_L	–	R	Bit[7:0]: tpm_value[7:0] Read out TPM value

5.16 LVDS interface [P9:0x00 - P9:0x0E]

table 5-16 LVDS interface registers (sheet 1 of 2)

address	register name	default value	R/W	description
P9:0x00	R0	0x2A	RW	Bit[7]: Two sync code enable in lane8 mode Bit[6]: Sync code manual mode enable Bit[5]: Sync code enable when only one lane Bit[4]: lvds_pclk_inv Bit[3]: Channel ID enable in sync code per lane mode Bit[2]: Not used Bit[1]: SAV first enable Bit[0]: Sync code mode 0: Split 1: Per lane
P9:0x01	RSVD	–	–	Reserved
P9:0x02	R2	0x00	RW	Bit[7:0]: Dummy data0[15:8]
P9:0x03	R3	0x80	RW	Bit[7:0]: Dummy data0[7:0]
P9:0x04	R4	0x00	RW	Bit[7:0]: Dummy data1[15:8]
P9:0x05	R5	0x10	RW	Bit[7:0]: Dummy data1[7:0]

table 5-16 LVDS interface registers (sheet 2 of 2)

address	register name	default value	R/W	description
P9:0x06	R6	0xAA	RW	Bit[7:0]: frame_start sync code in manual sync code mode
P9:0x07	R7	0x55	RW	Bit[7:0]: frame_end sync code in manual sync code mode
P9:0x08	R8	0x99	RW	Bit[7:0]: line_start sync code in manual sync code mode
P9:0x09	R9	0x66	RW	Bit[7:0]: line_end sync code in manual sync code mode
P9:0x0A	RA	0x00	RW	Bit[7:3]: Not used Bit[2]: r_hts_man_en Bit[1]: r_ln2_sel Bit[0]: r_chk_pcnt
P9:0x0B	RB	0x00	RW	Bit[7:4]: Not used Bit[3:0]: r_blk_times[11:8]
P9:0x0C	RC	0x00	RW	Bit[7:0]: r_blk_times[7:0]
P9:0x0D	RD	0x00	RW	Bit[7:0]: hts_man[15:8]
P9:0x0E	RE	0x00	RW	Bit[7:0]: hts_man[7:0]

5.17 page selection [0xFD]

table 5-17 page selection register

address	register name	default value	R/W	description
0xFD	PAGE_FLD_D2	0x00	RW	Bit[7:6]: mem_flag_w Bit[5:4]: mem_flag_r Bit[3:0]: Page select 0000: Page0 0001: Page1 0010: Page2 0100: OTP 0110: TPM 1001: LVDS Others: Not Used

6 operating specifications

6.1 absolute maximum ratings

table 6-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +125°C
supply voltage (with respect to ground)	AVDD	4.5V
	EXT_DVDD, EXT_EVDD	3V
	DOVDD	4.5V
all input/output voltages (with respect to ground)		-0.3V to DOVDD + 1V
I/O current on any input or output pin		± 200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

6.2 functional temperature

table 6-2 functional temperature

parameter	range
operating temperature (for applications up to 90 fps)[a]	-30°C to +85°C junction temperature
stable image temperature[b]	-20°C to +60°C junction temperature

a. sensor functions, but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range

6.3 DC characteristics

note Typical values for active (operating) current and standby current are estimated values and are subject to change when measured data using real silicon is available.

table 6-3 DC characteristics (-30°C < T_J < 85°C)

symbol	parameter	min	typ	max	unit
supply					
AVDD	supply voltage (analog and PLL)	2.7	2.8	2.9	V
DOVDD	supply voltage (digital I/O)	1.7	1.8	1.9	V
EXT_DVDD	supply voltage (digital circuits)	1.14	1.2	1.3	V
EXT_EVDD	supply voltage (MIPI core)	1.14	1.2	1.3	V
I_{AVDD}	active (operating) current		19	TBD	mA
I_{DOVDD}			0.7	TBD	mA
$I_{EXT\_DVDD} + I_{EXT\_EVDD}$			40	TBD	mA
$I_{AVDD\_STANDBY}$[a]	standby current[b]		1.9	TBD	µA
$I_{DOVDD\_STANDBY}$			0	TBD	µA
$I_{EXT\_DVDD\_STANDBY} + I_{EXT\_EVDD\_STANDBY}$			0.8	TBD	µA
internally derived voltages[c]					
VH	positive reference voltage	3		3.75	V
VN1	negative reference voltage 1	-2		-1	V
VN2	negative reference voltage 2	-2		-1	V
digital inputs (typical conditions: AVDD = 2.8V, DOVDD = 1.8V, EXT_DVDD = 1.2V, EXT_EVDD = 1.2V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[d]	SCL and SDA			0.54	V
V_{IH}[d]	SCL and SDA	1.26			V

a. standby current without input clock
b. standby current based on room temperature
c. not to be connected to external devices, except for adjacent capacitors
d. based on DOVDD = 1.8V

6.4 timing characteristics

figure 6-1 reference clock input timing diagram

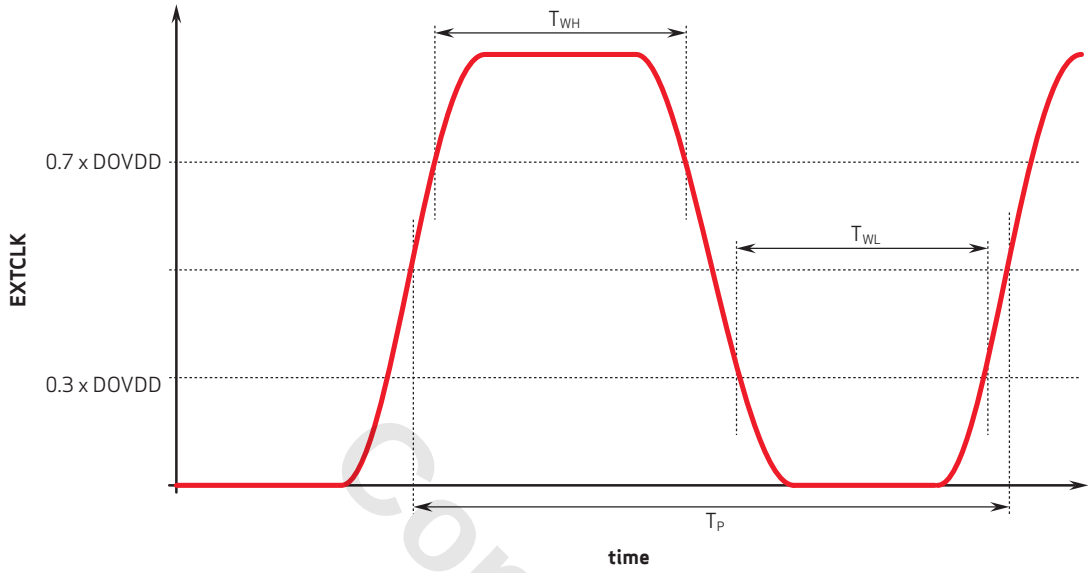


table 6-4 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
F_{EXTCLK}	frequency (EXTCLK)	6	24	27	MHz
T_P	period (EXTCLK)	37.0	41.7	166.7	ns
T_{WL}	low level width (EXTCLK)	$0.35 \times T_P$		$0.65 \times T_P$	ns
T_{WH}	high level width (EXTCLK)	$0.35 \times T_P$		$0.65 \times T_P$	ns

7 mechanical specifications

7.1 physical specifications

figure 7-1 package specifications

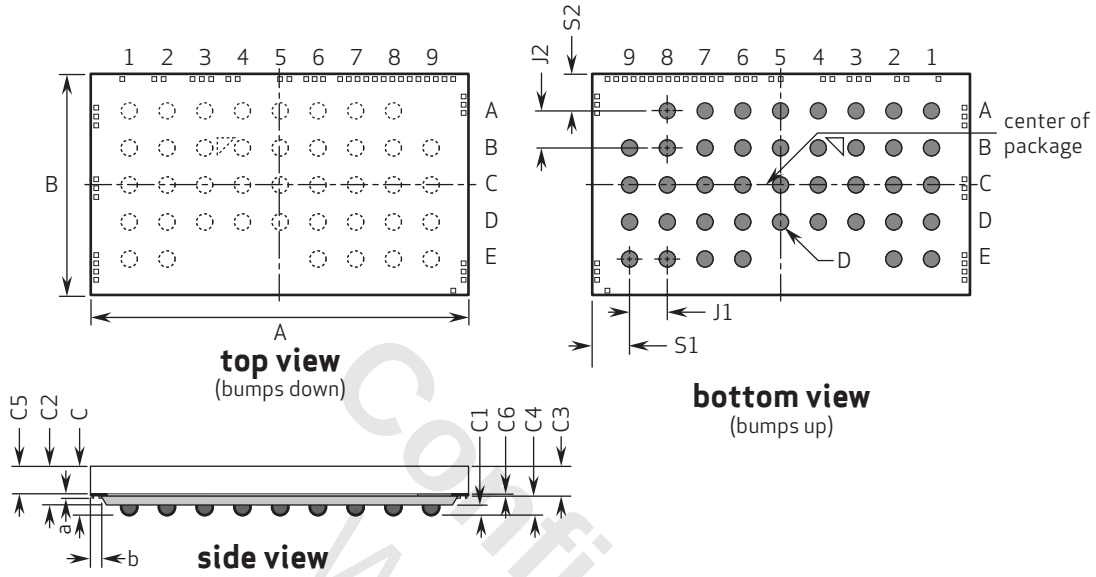


table 7-1 package dimensions (sheet 1 of 2)

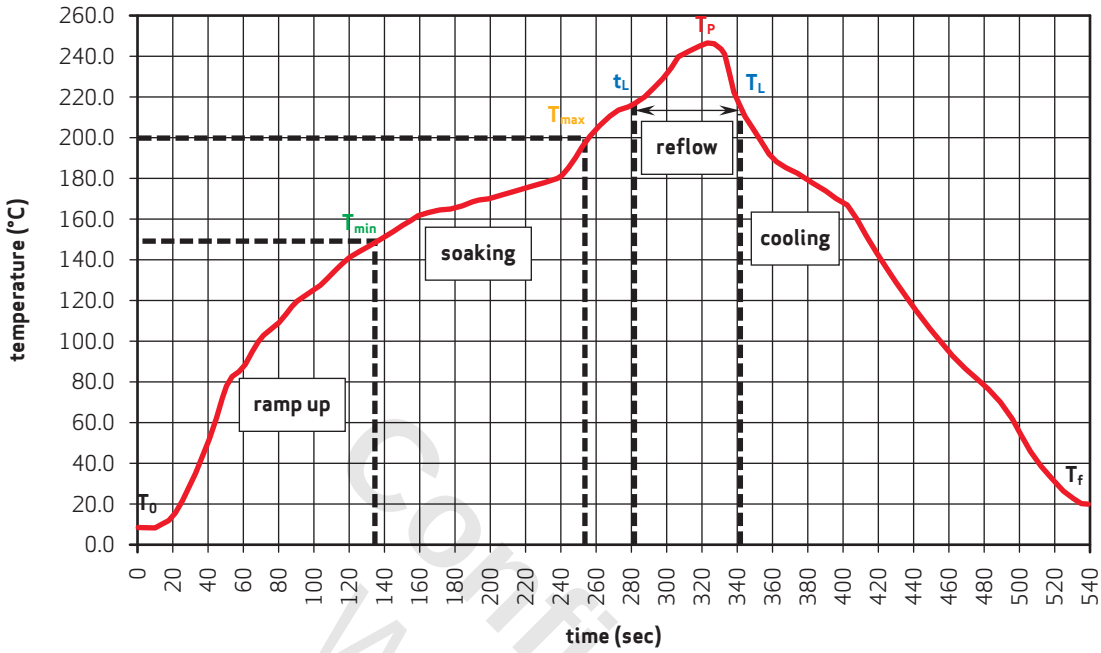
parameter	symbol	min	typ	max	unit
package body dimension x	A	6542.7	6567.7	6592.7	µm
package body dimension y	B	3913.8	3938.8	3963.8	µm
package height	C	575	630	685	µm
ball height	C1	100	130	160	µm
package body thickness	C2	470	500	530	µm
thickness from top glass surface to die	C3	330	345	360	µm
image plane height	C4	240	285	330	µm
glass thickness	C5	290	300	310	µm
air gap between sensor and glass	C6	41	45	49	µm
ball diameter	D	220	250	280	µm
total pin count	N		41		

table 7-1 package dimensions (sheet 2 of 2)

parameter	symbol	min	typ	max	unit
pin count x-axis	N1		9		
pin count y-axis	N2		5		
pins pitch x-axis	J1	650	660	670	µm
pins pitch y-axis	J2	650	660	670	µm
edge-to-pin center distance along x1	S1	613.9	643.85	673.9	µm
edge-to-pin center distance along y1	S2	619.4	649.4	679.4	µm
via depth	a	35	40	45	µm
edge-to-trench bottom opening distance along x and y	b	132	152	172	µm

7.2 IR reflow specifications

figure 7-2 IR reflow ramp rate requirements



note The OS02H10 uses a lead-free package.

note To reduce image artifacts from infrared light and to provide the best image quality. OmniVision recommends an IR cut filter.

table 7-2 reflow conditions[ab]

zone	description	exposure
ramp up A (T_0 to T_{min})	heating from room temperature to 150°C	temperature slope ≤ 3°C per second
soaking	heating from 150°C to 200°C	90 ~ 150 seconds
ramp up B (t_L to T_P)	heating from 217°C to 245°C	temperature slope ≤ 3°C per second
peak temperature	maximum temperature in SMT	245°C +0/-5° (duration max 30 sec)
reflow (t_L to T_L)	temperature higher than 217°C	30~120 seconds
ramp down A (T_P to T_L)	cooling down from 245°C to 217°C	temperature slope ≤ 3°C per second
ramp down B (T_L to T_f)	cooling down from 217°C to room temperature	temperature slope ≤ 2°C per second
T_0 to T_P	room temperature to peak temperature	≤ 8 minutes

a. maximum number of reflow cycles = 3

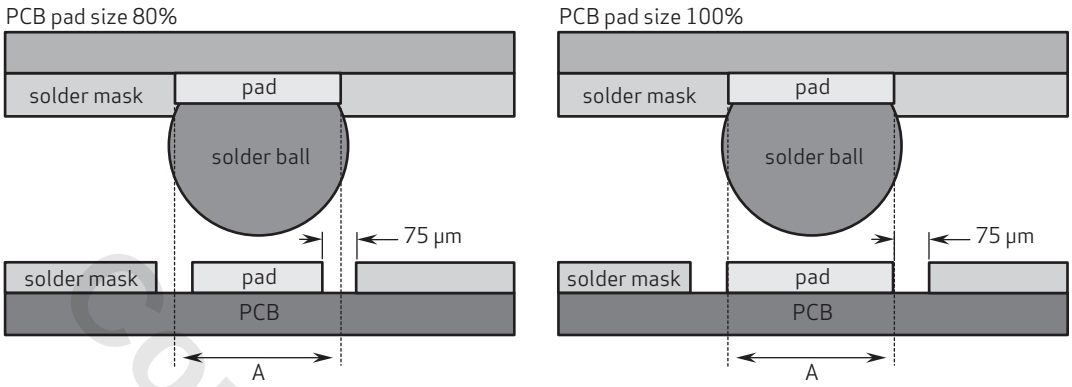
b. N2 gas reflow or control O2 gas PPM <500 as recommendation

7.3 PCB and SMT design recommendations

7.3.1 PCB design recommendations

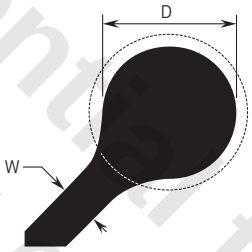
- solder pad of PCB: non solder mask defined (NSMD)
- PCB pad size: 80%~100% (90% ± 10%) of package's ball pad opening
- gap between pad to neighboring solder mask: 75 µm (minimum)

figure 7-3 PCB pad example



- trace width: must be less than 1/2 ball diameter (W<1/2 D)
- recommend adding tear drop design on trace connecting to via and pad

figure 7-4 tear drop design example



- PCB material: high performance FR4 with high Tg and low CTE substrate material is recommended
- package edge to PCB edge minimum 1.0 mm is recommended

table 7-3 ball pad opening size and recommended PCB NSMD ball pad size

device name	package type	package size	CSP/BGA ball pad opening size	recommended PCB NSMD ball pad size
OS02H10	CSP	6.5677 mm × 3.9388 mm	250 µm	225 µm ± 25 µm

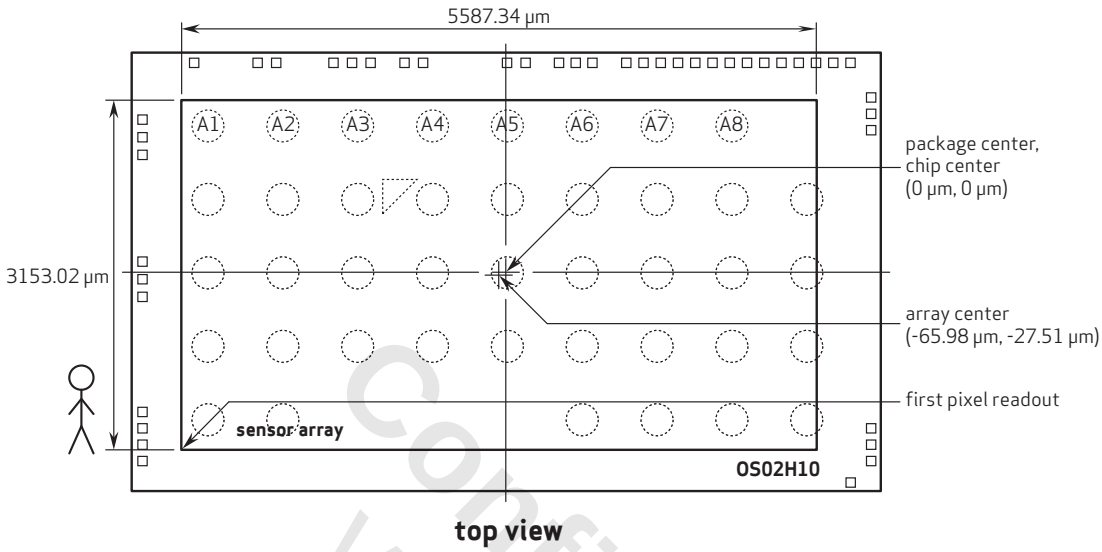
7.3.2 SMT design recommendations

- stencil: laser cut with electro-polishing
- stencil opening: 90~100% of PCB pad size
- stencil thickness: 0.08~0.15 mm
- solder material: SAC 305 is recommended
- solder paste: type 4 (20 µm to 38 µm) or finer solder sphere particle size is recommended
- SMT profile: refer to solder paste datasheet and product datasheet

8 optical specifications

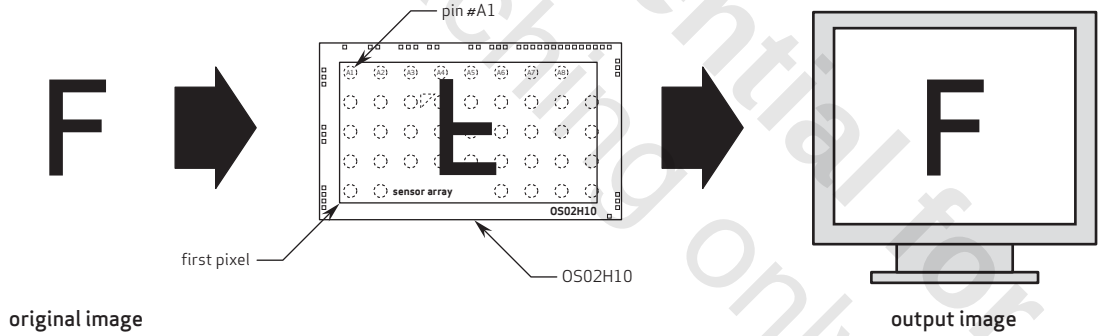
8.1 sensor array center

figure 8-1 sensor array center



note this drawing is not to scale and is for reference only.

figure 8-2 final image output



8.2 lens chief ray angle (CRA)

figure 8-3 chief ray angle (CRA)

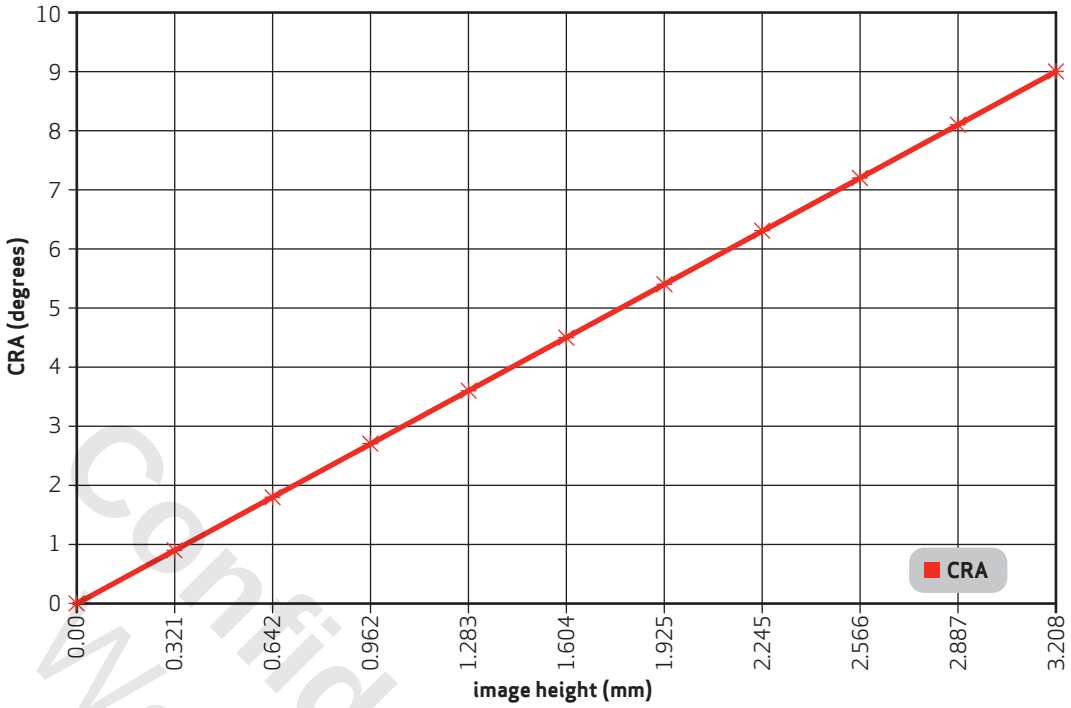


table 8-1 CRA versus image height plot

field (%)	image height (mm)	CRA (degrees)
0	0.00	0.00
10	0.321	0.90
20	0.642	1.80
30	0.962	2.70
40	1.283	3.60
50	1.604	4.50
60	1.925	5.40
70	2.245	6.30
80	2.566	7.20
90	2.887	8.10
100	3.208	9.00

revision history

version 1.0 09.03.2020

- initial release

version 1.1 11.17.2020

- on cover and in page headers, changed title to "...HD image sensor with PureCel®Plus and Nyxel® technologies"
- in features, changed first bullet to "supports image sizes: 1920x1080, 960x540, 960x540, and 480x270" and removed eleventh bullet
- in key specifications, changed active power requirement specification to <110 mW, added XSHUTDOWN power requirement specification, and changed output interfaces specification to "MIPI 1/2-lane / LVDS"
- in figure 1-1, changed signal names of pins A7, B7, C5, and C6 to "NC"
- in table 1-1, changed description of pin A4 to "MIPI/PLL digital circuits", and changed signal name, pin type, and description of pins A7, B7, C5 and C6 to "NC", "–", and "no connect", respectively
- in table 1-2, changed symbols in ninth row to "MCP, MCN, MDP0, MDN0, MDP1, MDN1"
- in figure 2-1, removed block under MIPI block from image output interface
- in figure 2-2, changed title to "OS02H10 reference schematic", changed pins A7, B7, C5, and C6 of U2 to NC, changed pins 8, 38 and 40 of J7 to no connect, removed U9 circuitry, and changed note 1 to "client platform provides four power supplies for AVDD, DOVDD, DVDD and EVDD; AVDD is connected to 2.8V power supply, DOVDD is compatible with 1.8V power supply, DVDD is connected to 1.2V power supply, and when using MIPI interface, EVDD is connected to 1.2V power supply; VH, VN1, and VN2 are all externally connected with a 1µF capacitor and then grounded without being led out to interface."
- in section 2.3, changed first sentence to "The OS02H10 supports RAW RGB output with a 2-lane MIPI interface." and removed table 2-2
- in section 2.5, changed first sentence to "MIPI and LVDS data output interfaces are all integrated inside the OS02H10 sensor." and removed section 2.5.1
- in section 4.7, changed last sentence of third paragraph to "HTS is the horizontal total size that can be read by registers {P1:0xDA, P1:0xDB}."
- in table 4-11, changed address of register name HTS_8MSB to P1:0xDA and changed address of register name HTS_8LSB to 0xDB
- in table 5-1, changed register name, default value, R/W, and description of registers P0:0x33~P0:0x36 to "RSVD", "–", "–", and "Reserved", respectively, changed register name of register P0:0x52 to "OSC_CLK_DIV_GATING_BUF, PLL_CLK_OSC_GATING_BUF", changed description of register bits P0:0x52[7:5] and P0:0x52[2:0] to "Not used", and changed register name, default value, R/W, and description of registers P0:0x6F~P0:0x71 to "RSVD", "–", "–", and "Reserved", respectively
- in section 5.5, changed title to "CIS control [P1:0x01 ~ P1:0x4F, P1:0xCD ~ P1:0xF2]"
- in table 5-5, removed rows for P1:0xDA (HS_PERIOD_NUM_5MSB) and P1:0xDB (HS_PERIOD_8LSB), changed address of register name HTS_8MSB from P1:0x8C to P1:0xDA changed address of register name HTS_8LSB from 0x8D to 0xDB, and changed register name,

default value, R/W, and description of register P1:0xF0 to "RSVD", "–", "–", and "Reserved", respectively

- in chapter 5, removed section 5.16
- in table 5-17 (previously table 5-18), removed binary value selection 0111 from description of register bits 0xFD[3:0]
- in section 6.3, added sidebar note, "Typical values for active (operating) current and standby current are estimated values and are subject to change when measured data using real silicon is available."
- in table 6-3, changed parameter for supply symbol EXT_EVDD to "supply voltage (MIPI core)", removed row for supply symbol I_{EXT_EVDD}, changed supply symbol I_{EXT_DVDD} to "I_{EXT_DVDD} + I_{EXT_EVDD}", removed supply symbol $I_{EXT\_EVDD\_STANDBY}$, changed supply symbol $I_{EXT\_DVDD\_STANDBY}$ to "$I_{EXT\_DVDD\_STANDBY}$ + $I_{EXT\_EVDD\_STANDBY}$", changed typ values for supply symbols I_{AVDD}, I_{DOVDD}, and I_{EXT_DVDD} + I_{EXT_EVDD} to 19 mA, 0.7 mA, and 40 mA, respectively, changed typ values for supply symbols $I_{AVDD\_STANDBY}$, $I_{DOVDD\_STANDBY}$, and $I_{EXT\_DVDD\_STANDBY}$ + $I_{EXT\_EVDD\_STANDBY}$ to 1.9 µA, 0 µA, and 0.8 µA, respectively, and removed table footnote a

Future in Sight®

OmniVision Technologies, Inc.

UNITED STATES

4275 Burton Drive
Santa Clara, CA 95054
tel: +1 408 567 3000
Chicago +1 847 508 0217
Detroit +1 248 919 6900
Optics Division +1 303 449 5593

UNITED KINGDOM

Hants +44 1252 761601

GERMANY

Munich +49 89 6381 9988

CHINA

Shanghai + 86 21 6175 9888
+86 21 6154 8000
Beijing + 86 10 8642 4200
Shenzhen + 86 755 8435 9733
Wuhan +86 27 5975 7800
Xian +86 29 8885 2537

INDIA

Bangalore +91 80 4112 8966

KOREA

Seoul + 82 2 3472 3769

JAPAN

Yokohama +81 45 478 7977
Kyoto +81 75 708 5352

NORWAY

Oslo +47 2295 8100

SINGAPORE +65 6933 1933

TAIWAN

Taipei +886 2 2657 9800
Hsin-chu +886 3 5656688

website: **www.ovt.com**